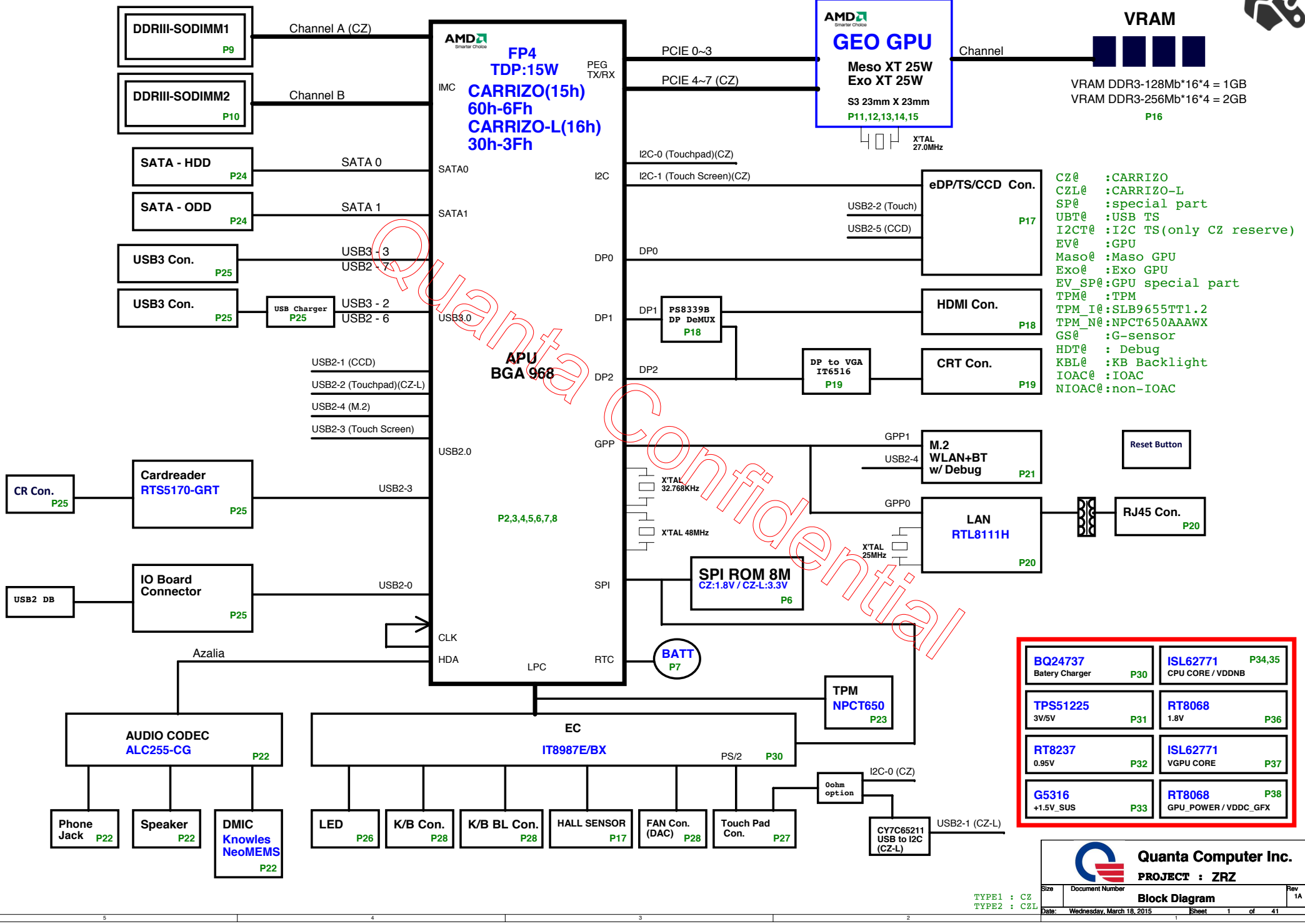
ZRZ/ZRZL BLOCK DIAGRAM




```
CZ@    :CARRIZO
CZL@   :CARRIZO-L
SP@    :special part
UBT@   :USB TS
I2CT@  :I2C TS(only CZ reserve)
EV@    :GPU
Maso@  :Maso GPU
Exo@   :Exo GPU
EV_SP@:GPU special part
TPM@   :TPM
TPM_I@:SLB9655TT1.2
TPM_N@:NPCT650AAAWX
GS@    :G-sensor
HDT@   : Debug
KBL@   :KB Backlight
IOAC@ :IOAC
NIOAC@:non-IOAC
```

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TYPE1 : CZ
TYPE2 : CZL

Quanta Computer Inc.
PROJECT : ZRZ
Size | Document Number: Block Diagram | Rev 1A
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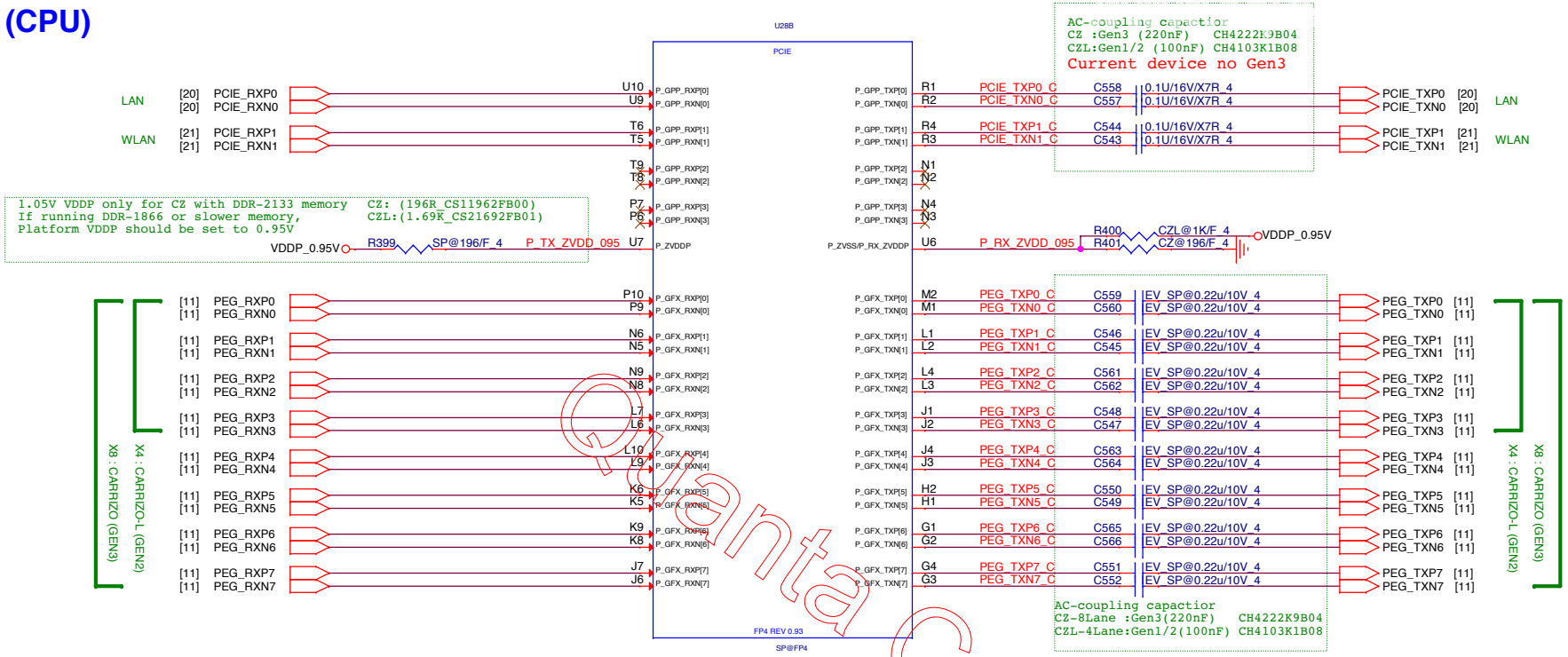
(CPU)



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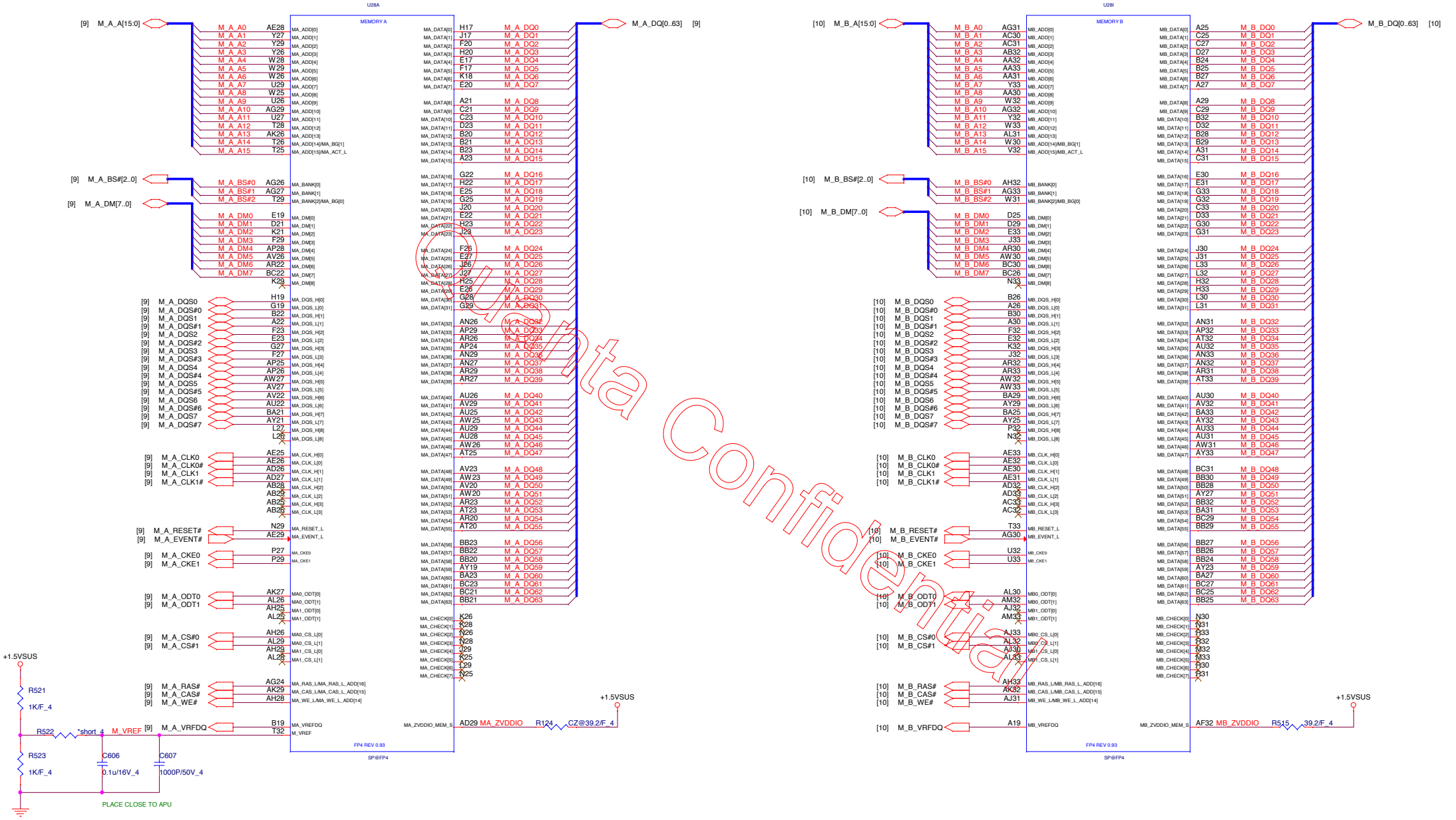
Quanta Computer Inc.		
PROJECT : ZRZ		
Size	Document Number: FP4 PCIE I/F(1/7)	Rev: 1A
Date: Friday, March 06, 2015	Sheet 2 of 41	

(CPU)

Channel A:CZ ONLY



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Quanta Computer Inc.

PROJECT : ZRZ

Size	Document Number	Rev
	FP4 DDR3 I/F(2/7)	1A
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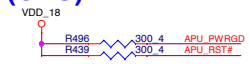
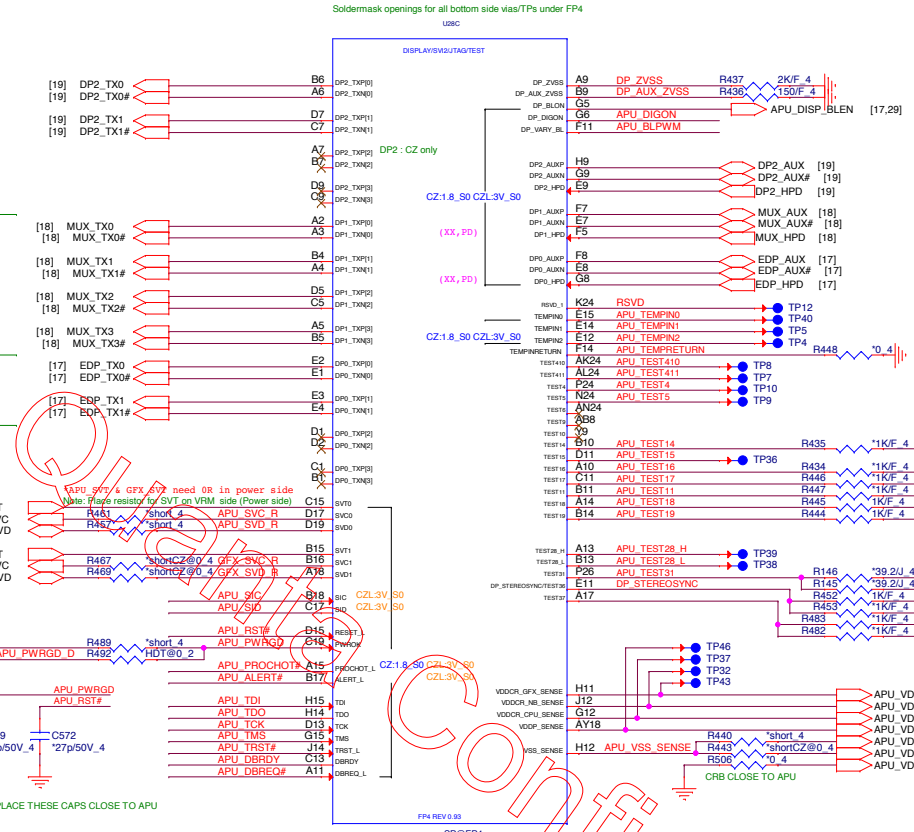
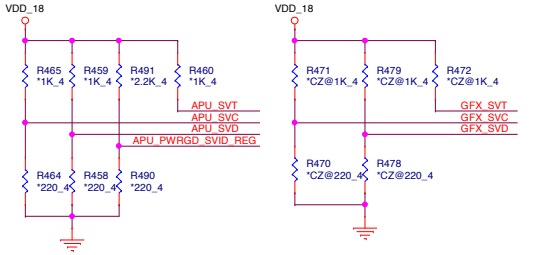
(CPU)



Soldermask openings for all bottom side vias/TPs under FP4



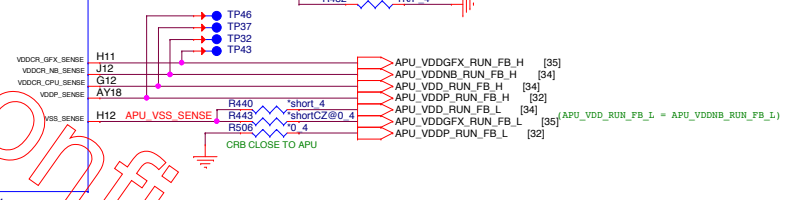
Serial VID

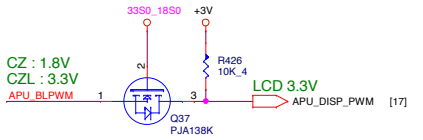


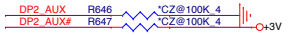
VFIX MODE — VID Override table (VDD)

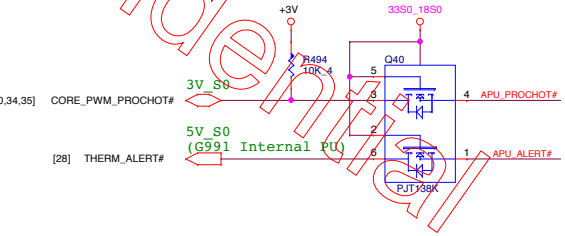
SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

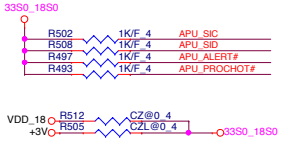
FOR DEBUG, PLACE THESE CAPS CLOSE TO APU



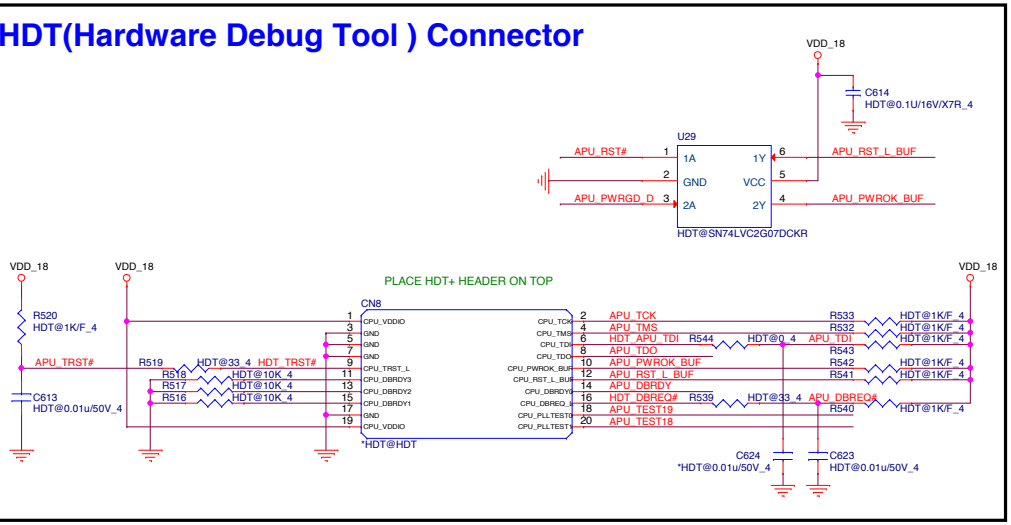




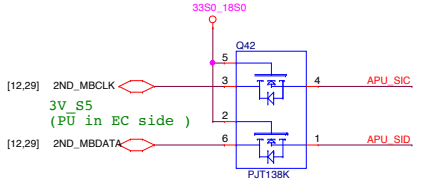




HDT(Hardware Debug Tool) Connector



SMBUS (Internal Thermal sensor)



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Quanta Computer Inc.
PROJECT : ZRZ

Size	Document Number	Rev
	FP4 DISPLAY/MISC(3/7)	1A
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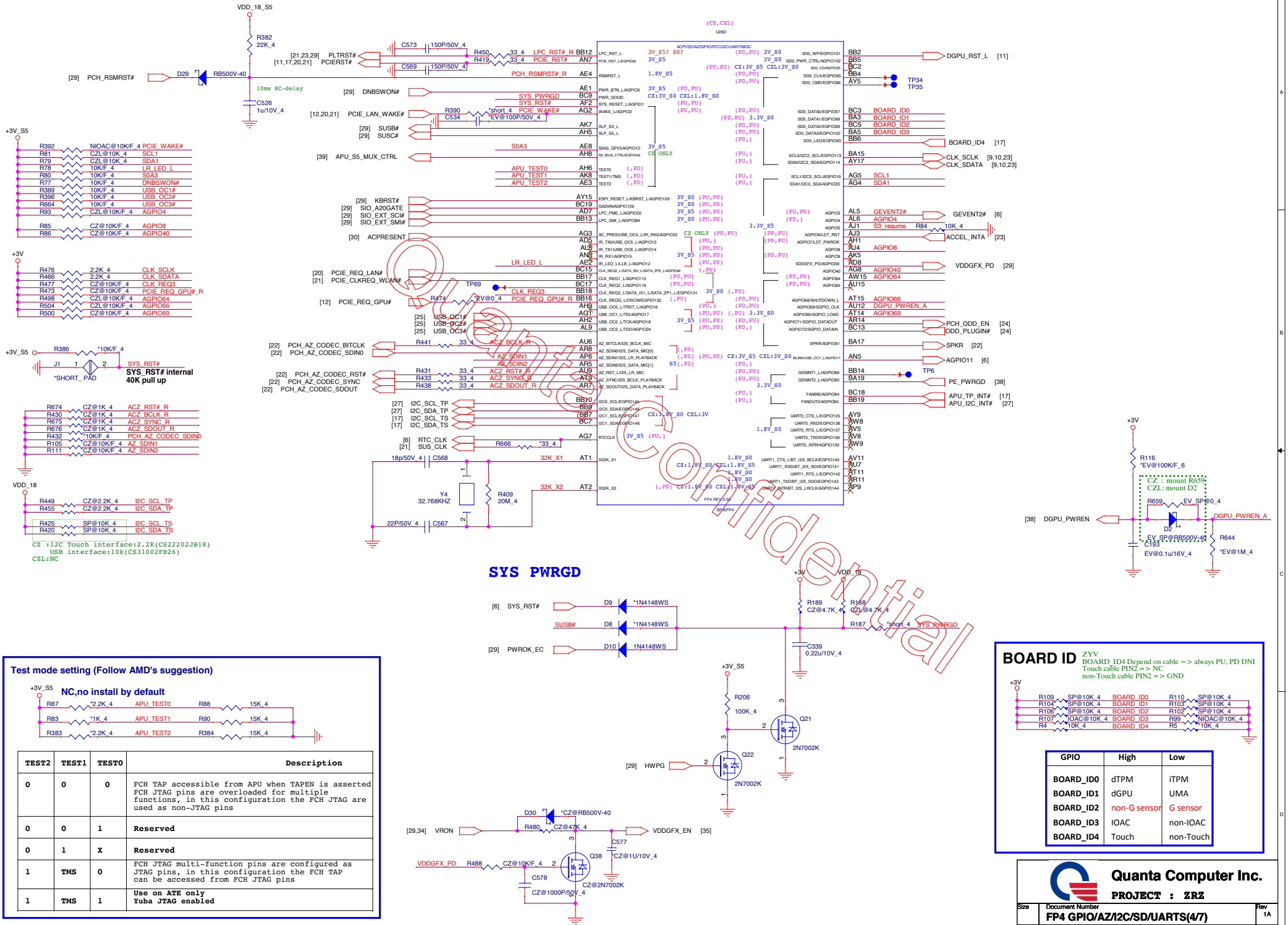
(CPU)



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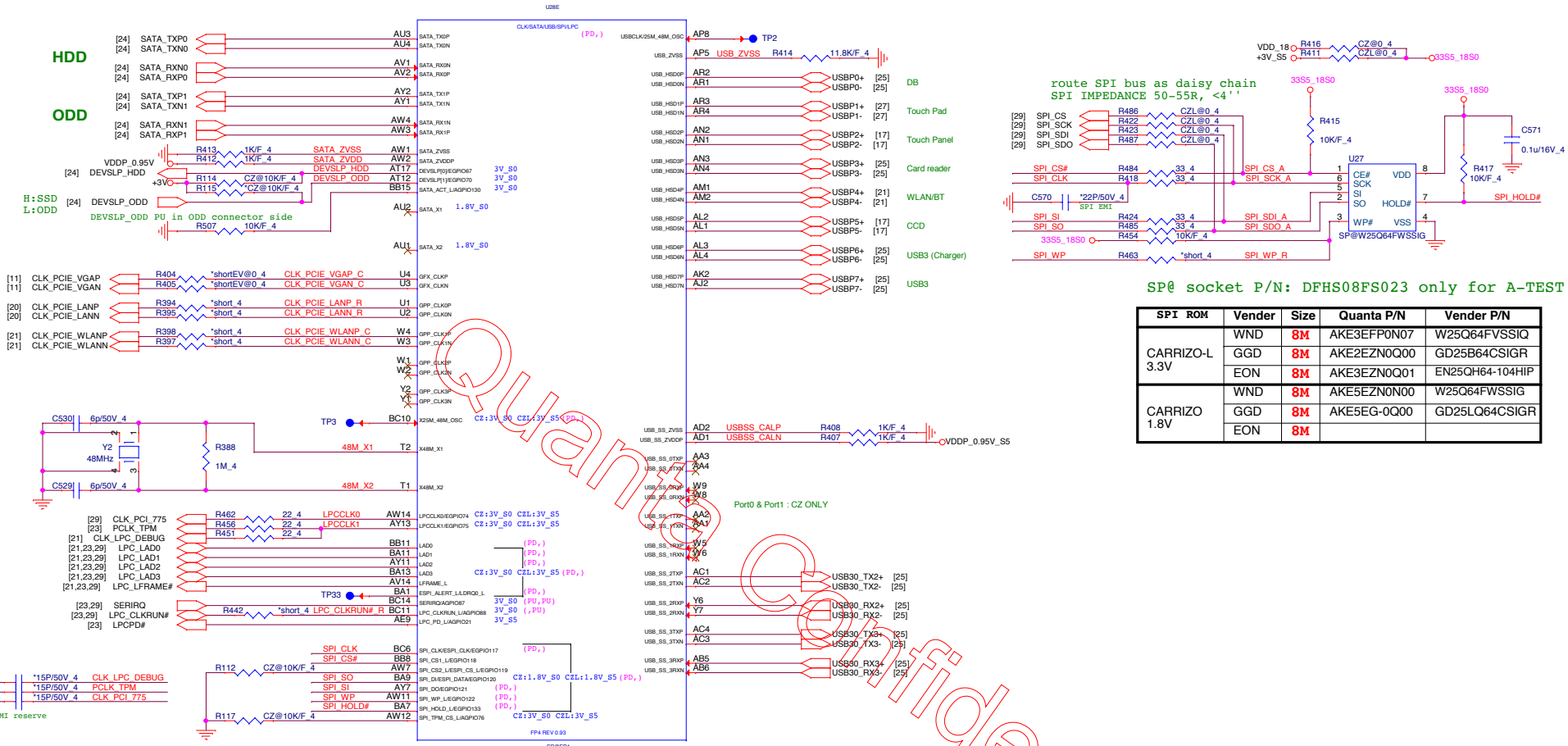
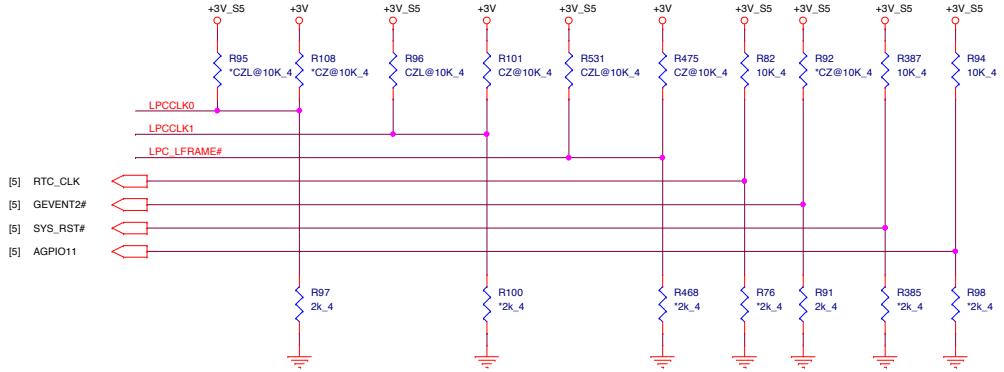
(CPU)



SPI ROM	Vender	Size	Quanta P/N	Vender P/N
CARRIZO-L 3.3V	WND	8M	AKE3EFP0N07	W25Q64FVSSIQ
	GGD	8M	AKE2EZN0Q00	GD25B64CSIGR
	EON	8M	AKE3EZN0Q01	EN25QH64-104HIP
CARRIZO 1.8V	WND	8M	AKE5EZN0N00	W25Q64FWSSIG
	GGD	8M	AKE5EG-0Q00	GD25LQ64CSIGR
	EON	8M		

STRAPS PINS



	LPC_CLK0	LPC_CLK1	LFRAME#	RTC_CLK (Int pull-up)	GEVENT2# (AGPIO3) (Int pull-up)		SYS_RST# (Int pull-up)	AGPIO11(BLINK) (Int pull-up)
					CZ-L	CZ		
PU	BOOT Fail Timer ENABLE	Internal CLKGEN DEFAULT	SPI ROM DEFAULT	Coin battery is on board. DEFAULT	1.8V SPI ROM	Enhanced Reset logic (faster resume from S5)	normal reset mode DEFAULT	LDT_RST#/LDT_PWRGD output to APU DEFAULT
PD	BOOT Fail Timer DISABLE DEFAULT	External CLKGEN	LPC ROM	Coin battery is not on board.	3.3V SPI ROM DEFAULT	Default to Traditional Reset logic DEFAULT	short reset mode	LDT_RST#/LDT_PWRGD output to Pads

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Size	Document Number FP4 SATA/USB/LPC/SPI(5/7)		Rev 1A
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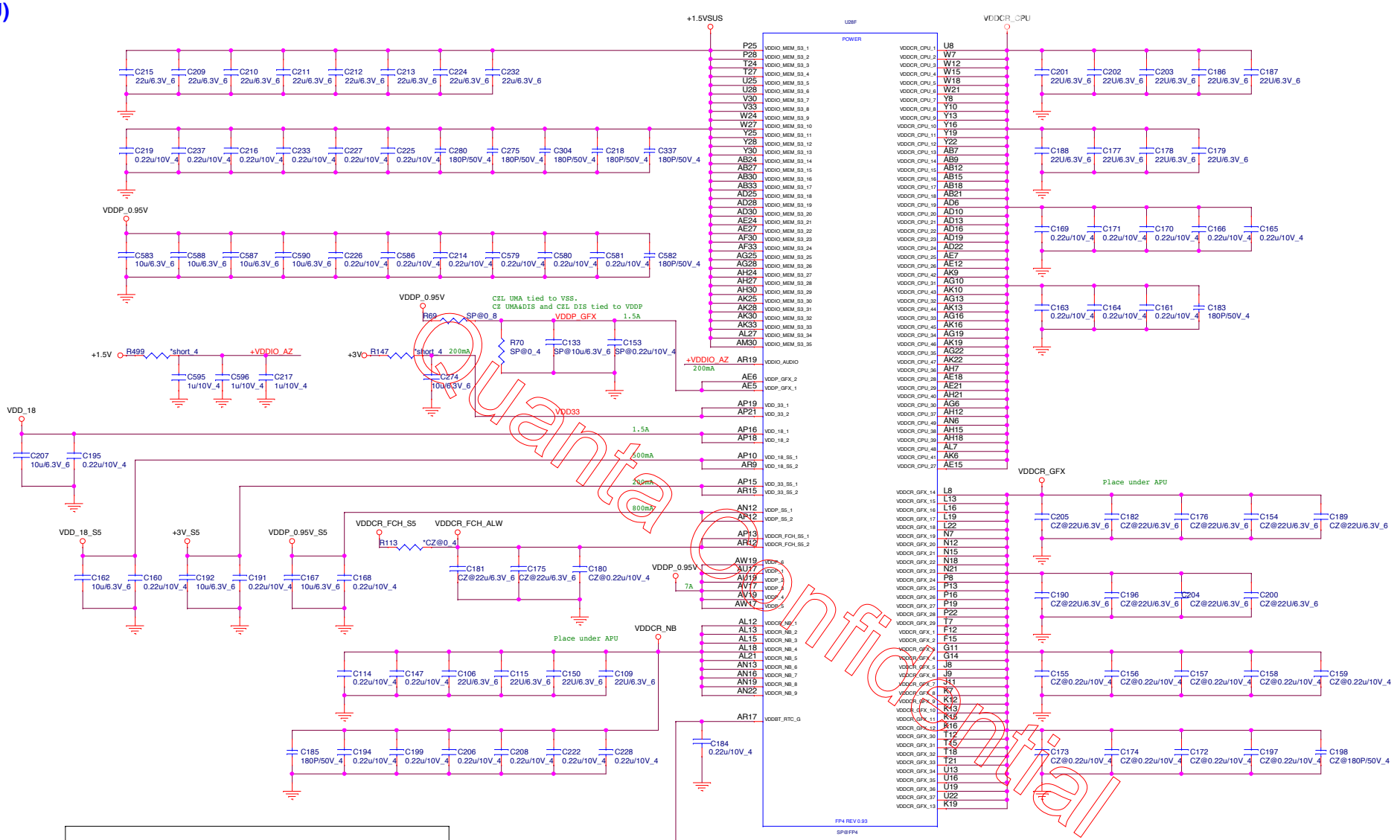
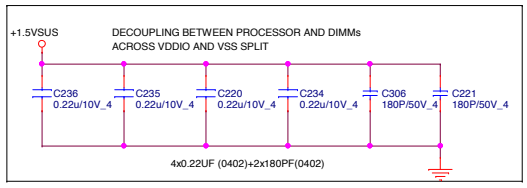
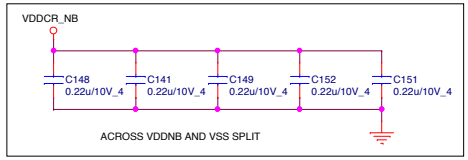
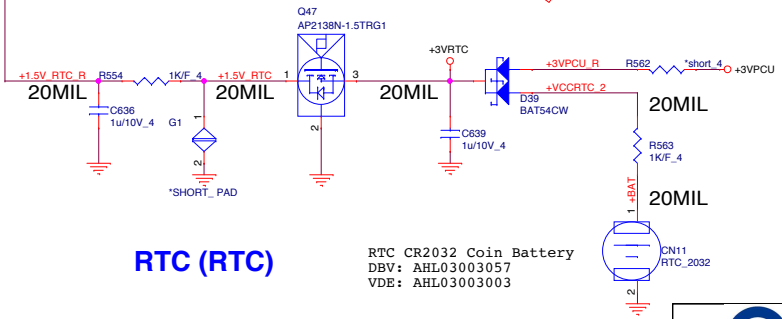
(CPU)









RTC (RTC)

RTC CR2032 Coin Battery
DBV: AHL03003057
VDE: AHL03003003

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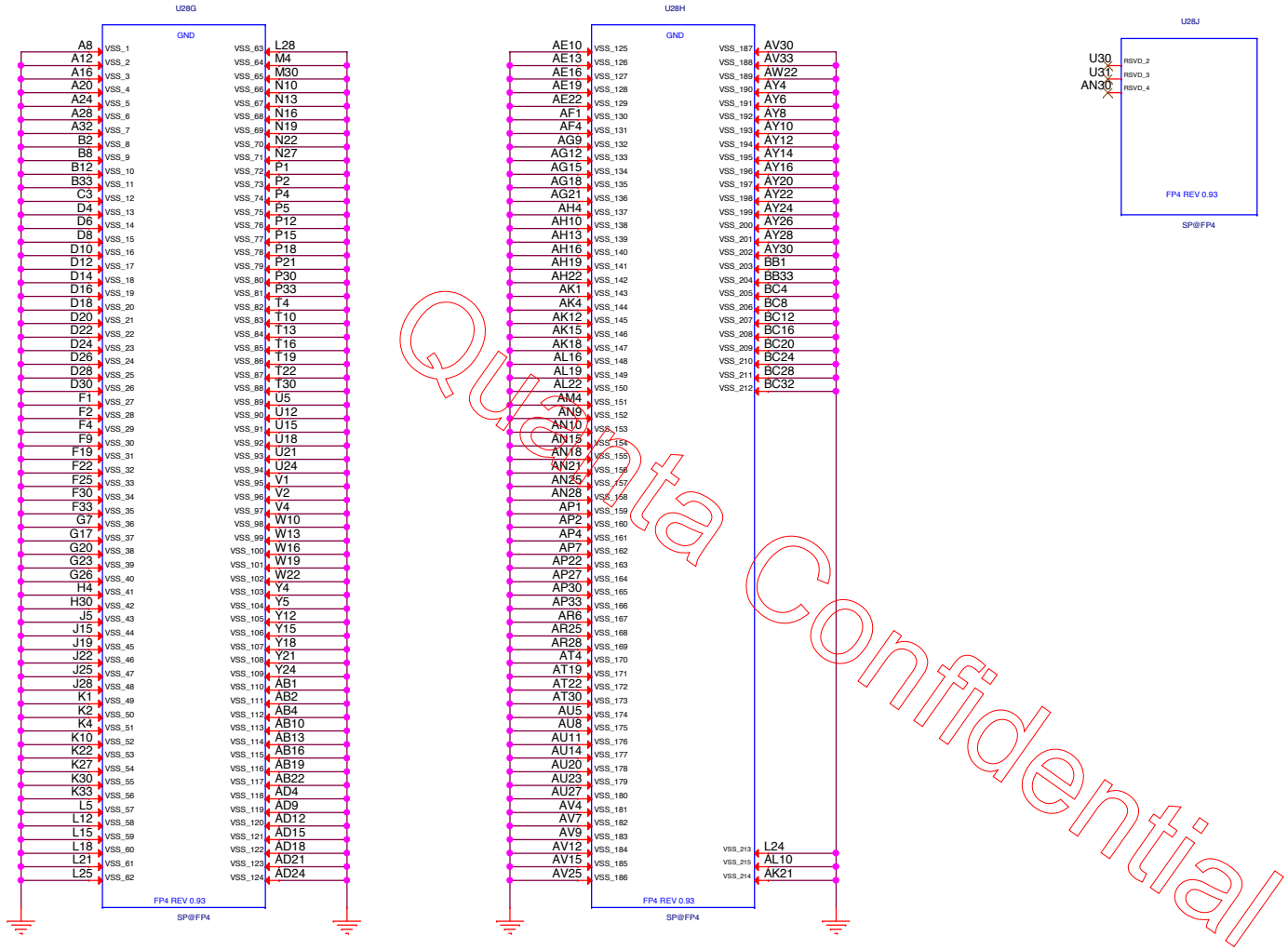
Quanta Computer Inc.		
PROJECT : ZRZ		
Size	Document Number: FP4 POWER(6/7)	Rev: 1A
Date: Wednesday, March 18, 2015	Sheet 7 of 41	

(CPU)



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PROJECT : ZRZ

Size	Document Number	Rev
	FP4 GND(7/7)	1A
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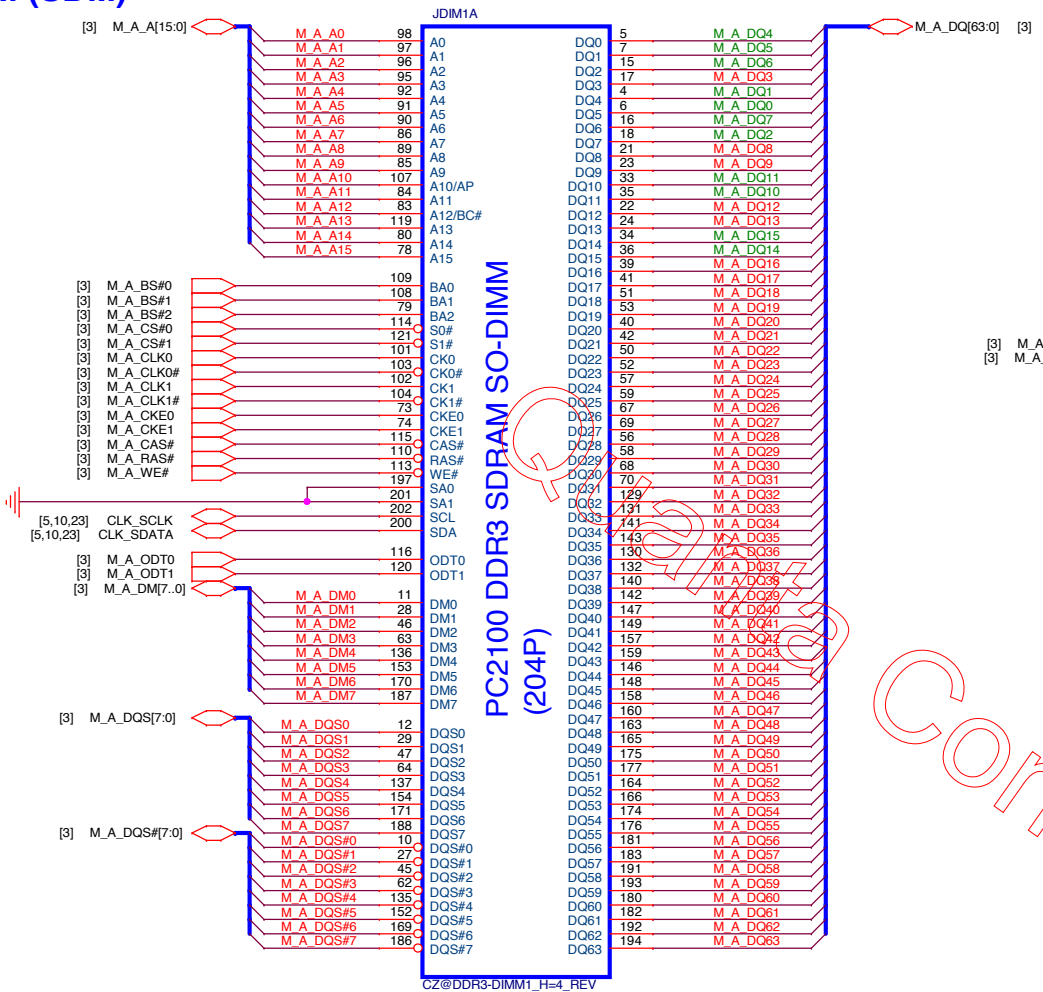
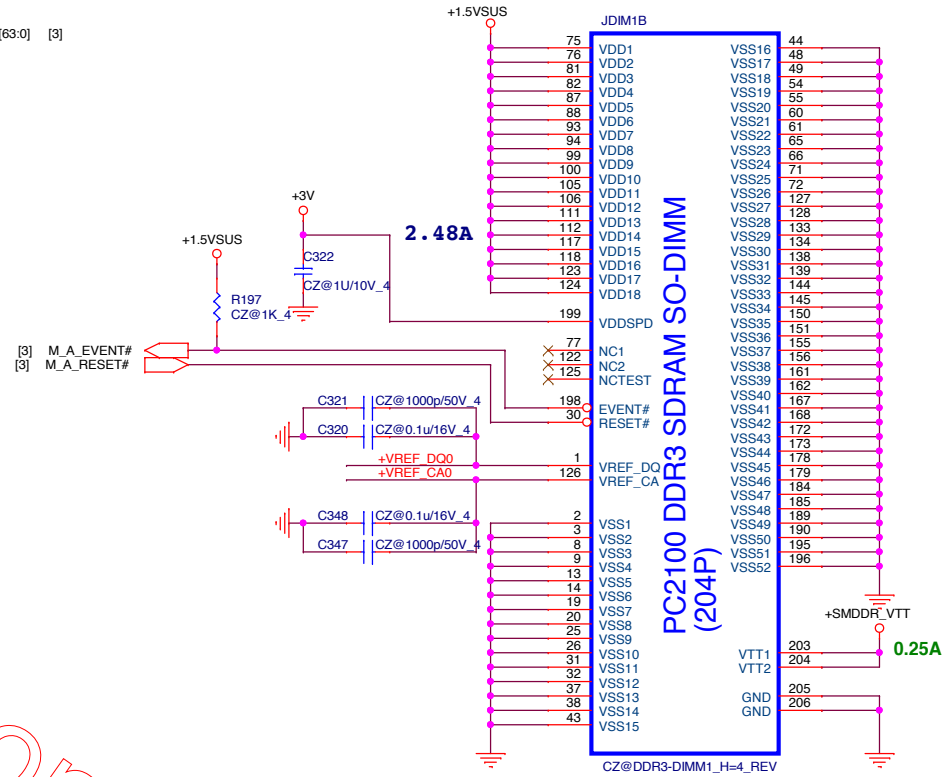
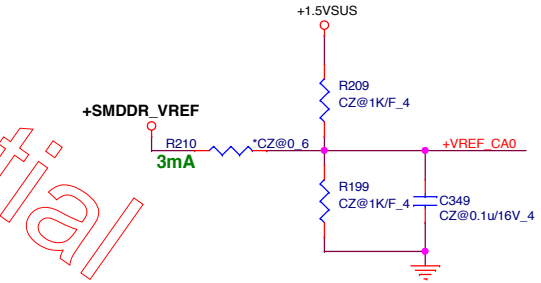
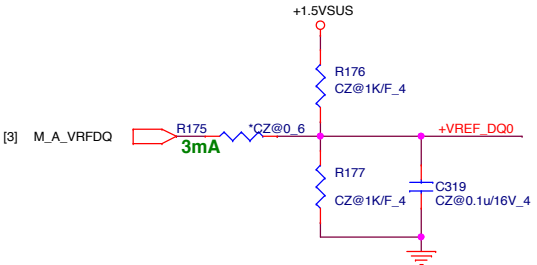
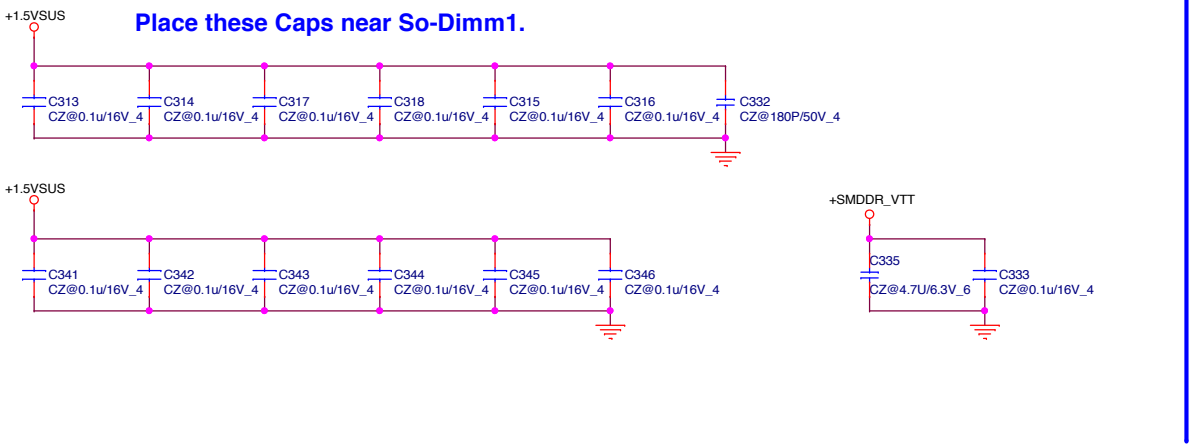
SODIMM (SDM)











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PROJECT : ZRZ

Size	Document Number	Rev
	DDR3 DIMM 1	1A
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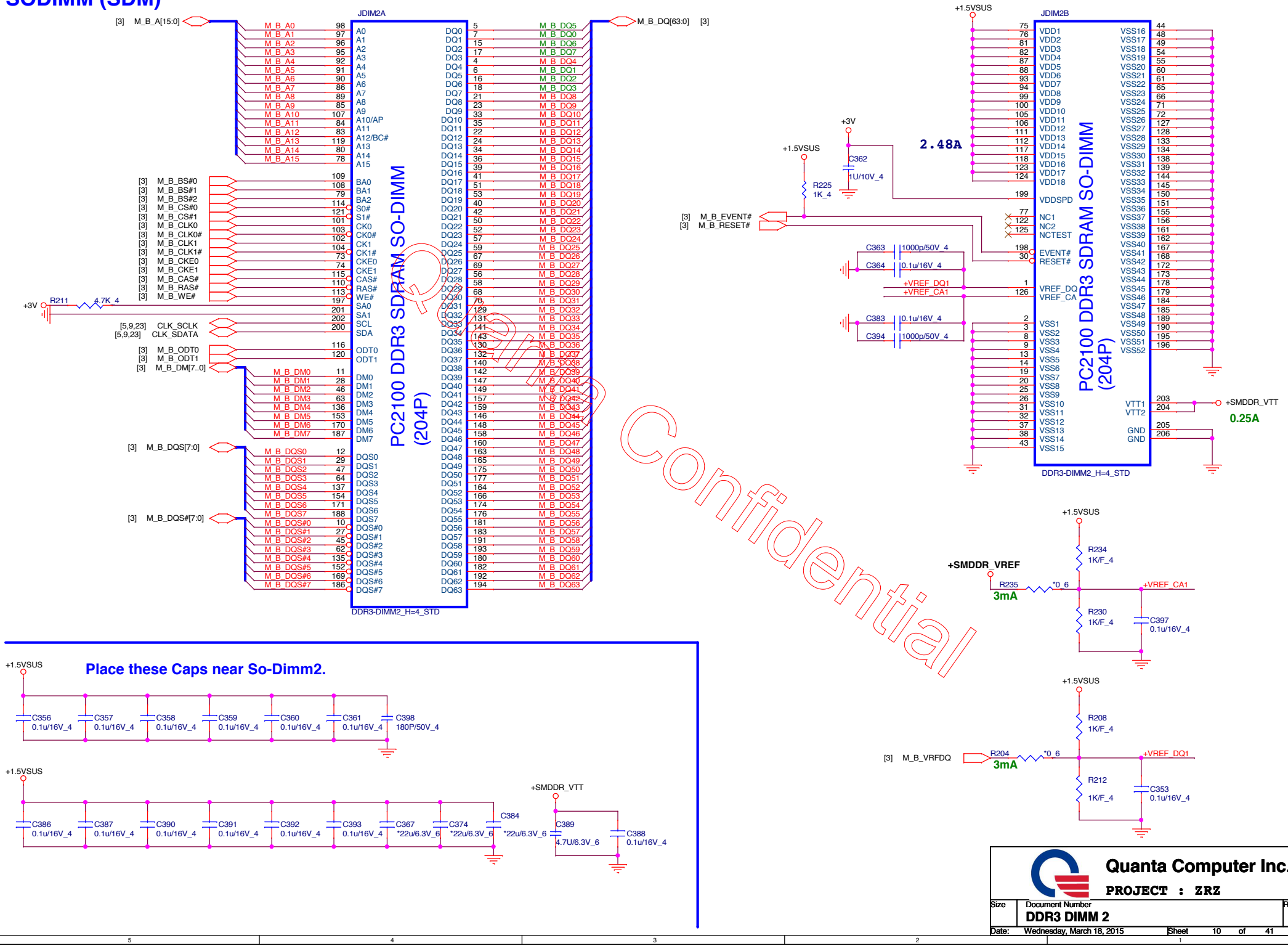
SODIMM (SDM)



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Place these Caps near So-Dimm2.

Quanta Computer Inc.			
PROJECT : ZRZ			
Size	Document Number		Rev
	DDR3 DIMM 2		1A
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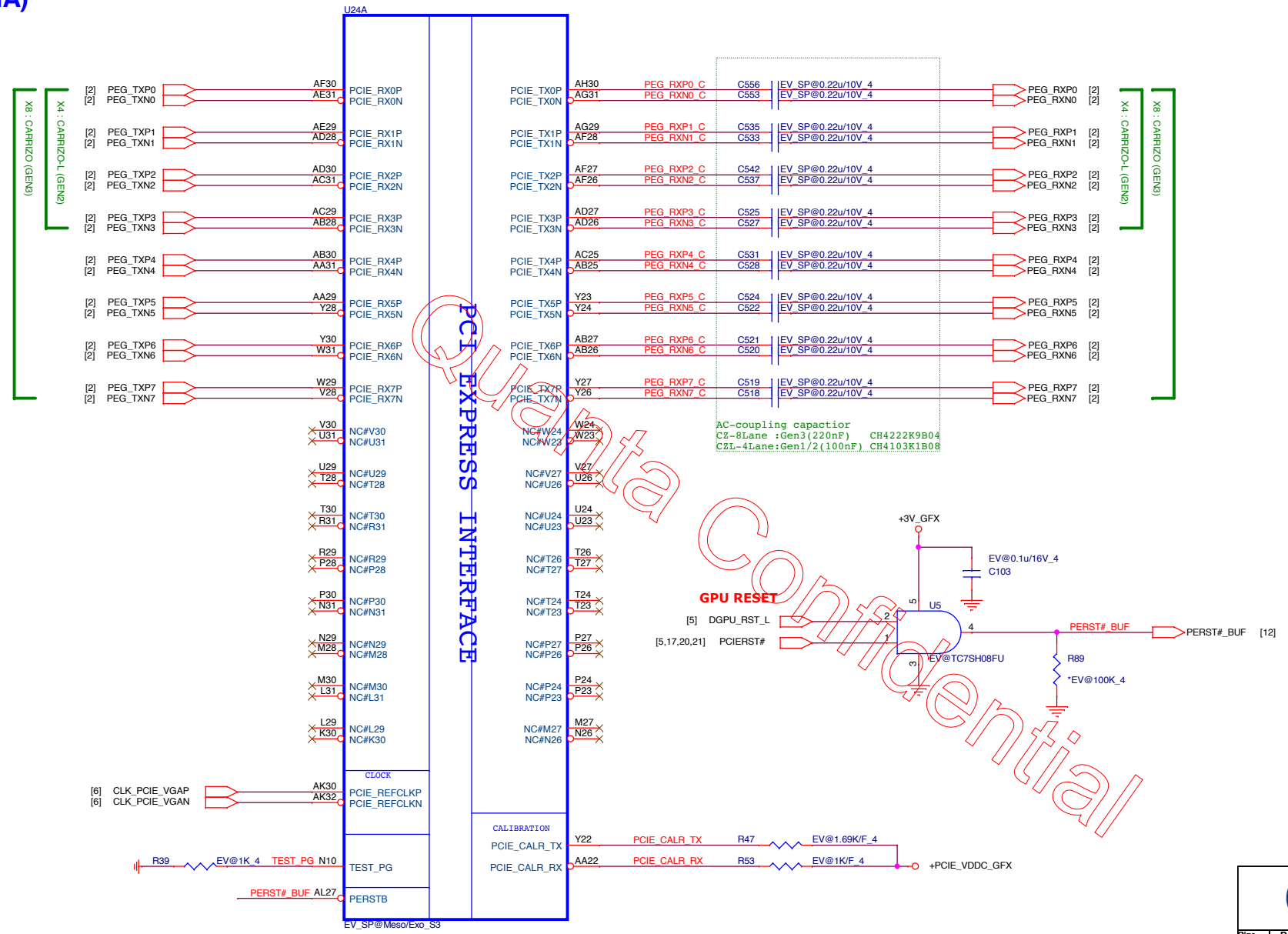
(VGA)



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PROJECT : ZRZ	
Size	Document Number: Meso/Exo_S3_PCIE(1/6) — Rev: 1A
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(VGA)

The SMBus slave ID is default 0x41

Meso SCL/SDA PU : 47k ohm (CS34702JB21)
Exo SCL/SDA PU: 45.3kohm (CS34532FB18)

PU/PD

AMD GAE:Debug port TDO left as floating.

ZYV not PU PEX_CLKREQ#

ZYV not PD TEMP_FAIL

Peak Current Control (PCC) GPIO_6.
FOR MESO ONLY

AMD GAE:GPIO_6 keep as unconnected, don't stuff the components on this relative circuitry

to power IC

to power IC

AMD GAE:CLKRFQ keep this pin as floating.

GPIO_11, 12, and 13 FOR MESO ONLY, EXO become NC

EXO MLPS setting PD
MEXO no mount

EXO ONLY: stuff Ra=> disable MLPS
stuff Rb=> enable MLPS

DP_VDDC

EXO	MESO
10u x1	1u x1
1u x1	0.1u x1
0.1u x1	

SVC	SVD	Output Voltage
0	0	1.1 Volts
0	1	1.0 Volts
1	0	0.9 Volts
1	1	0.8 Volts

Exo Boot

EXTERNAL THERMAL SENSOR

EXO Level Shift

to power IC

	EXO	MESO
PS0[5:1]	11001	11001
PS1[5:1]	11000	11001
PS2[5:1]	11000	11000
PS3[5:1]	11xxx	11xxx

PS_3[3:1]	Vendor	Type	Vendor P/N	R3pu	R3pd
000	Hynix 2G	256Mx16 *4,1000Mhz	H5TC4G63AFR-11C	NC	4.75K
001	Samsung 2G	256Mx16 *4,1000Mhz	K4W4G1646D-BC1A	8.45K	2K
010	Micro 2G	256Mx16 *4,1000Mhz	MT41J256M16HA-093G:E	4.53K	2K
011	Hynix 2G	256Mx16 *4,1000Mhz	H5TC4G63CFR-N0C	6.98K	4.99K

BIT[5:4]	C (nF)
00	680
01	82
10	10
11	NC

BIT[3:1]	Rpu	Rpd
000	NC	4750
001	8450	2000
010	4530	2000
011	6980	4990
100	4530	4990
101	3240	5620
110	3400	10000
111	4750	NC

PS_3 [5,4] should be 11 due to this is no output/audio design

GEN2(CZL):R75 NC
R71 4.75K(CS24752FB12)
GEN3(CZ) :R75 8.45K(CS28452FB12)
R71 2K(CS22002FB19)

Quanta P/N====>
4.53K: CS24532FB08 4.99K: CS24992FB26
6.98K: CS26982FB01 3.24K: CS23242FB17
5.62K: CS25622FB18 8.45K: CS28452FB12
4.75K: CS24752FB12 2K: CS22002FB19

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Quanta Computer Inc.	
PROJECT : ZRZ	
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(VGA)

U24E

AA27	PCIE_VSS#1	GND#1	A3
AB24	PCIE_VSS#2	GND#2	A30
AB32	PCIE_VSS#3	GND#3	AA13
AC24	PCIE_VSS#4	GND#4	AA16
AC26	PCIE_VSS#5	GND#5	AB10
AC27	PCIE_VSS#6	GND#6	AB15
AD25	PCIE_VSS#7	GND#7	AB6
AD32	PCIE_VSS#8	GND#8	AC9
AE27	PCIE_VSS#9	GND#9	AD6
AF32	PCIE_VSS#10	GND#10	AD8
AG27	PCIE_VSS#11	GND#11	AE7
AH32	PCIE_VSS#12	GND#12	AG12
K28	PCIE_VSS#13	GND#13	AH10
K32	PCIE_VSS#14	GND#14	AH28
L27	PCIE_VSS#15	GND#15	B10
M32	PCIE_VSS#16	GND#16	B12
N25	PCIE_VSS#17	GND#17	B14
N27	PCIE_VSS#18	GND#18	B16
P25	PCIE_VSS#19	GND#19	B18
P32	PCIE_VSS#20	GND#20	B20
R27	PCIE_VSS#21	GND#21	B22
T25	PCIE_VSS#22	GND#22	B24
T32	PCIE_VSS#23	GND#23	B26
U25	PCIE_VSS#24	GND#24	B6
U27	PCIE_VSS#25	GND#25	B8
V32	PCIE_VSS#26	GND#26	C1
W25	PCIE_VSS#27	GND#27	C32
W26	PCIE_VSS#28	GND#28	E28
W27	PCIE_VSS#29	GND#29	F10
Y25	PCIE_VSS#30	GND#30	F12
Y32	PCIE_VSS#31	GND#31	F14
		GND#32	F16
		GND#33	F18
		GND#34	F2
		GND#35	F20
		GND#36	F22
		GND#37	F24
		GND#38	F26
		GND#39	F6
		GND#40	F8
		GND#41	G10
		GND#42	G27
		GND#43	G31
		GND#44	G8
		GND#45	H14
		GND#46	H17
		GND#47	H2
		GND#48	H20
		GND#49	H6
		GND#50	J27
		GND#51	J31
		GND#52	K11
		GND#53	K2
		GND#54	K22
		GND#55	K6
		GND#84	T11
		GND#85	R11
M6	GND#56		
N11	GND#57		
N13	GND#58		
N16	GND#59		
N18	GND#60		
N21	GND#61		
P6	GND#62		
P9	GND#63		
R12	GND#64		
R15	GND#65		
R17	GND#66		
R20	GND#67		
T13	GND#68		
T16	GND#69		
T18	GND#70		
T21	GND#71		
T6	GND#72		
U15	GND#73		
U17	GND#74		
U20	GND#75		
U9	GND#76		
V13	GND#77		
V16	GND#78		
V18	GND#79		
Y10	GND#80		
Y15	GND#81		
Y17	GND#82	VSS_MECH#1	A32
Y20	GND#83	VSS_MECH#2	AM1
AA11	GND#86	VSS_MECH#3	AM32
M12	GND#87		
V11	GND#88		

GND

EV_SP@Meso/Exo_S3

U24F

LVDS CONTROL

NC_UPHYAB_TMDPA_TX0N	AL15
NC_UPHYAB_TMDPA_TX0P	AK14
NC_UPHYAB_TMDPA_TX1N	AH16
NC_UPHYAB_TMDPA_TX1P	AJ15
NC_UPHYAB_TMDPA_TX2N	AL17
NC_UPHYAB_TMDPA_TX2P	AK16
NC_UPHYAB_TMDPA_TX3N	AH18
NC_UPHYAB_TMDPA_TX3P	AJ17
NC_TXOUT_L3P	AL19
NC_TXOUT_L3N	AK18

TMDP

NC_UPHYAB_TMDPB_TX0N	AH20
NC_UPHYAB_TMDPB_TX0P	AJ19
NC_UPHYAB_TMDPB_TX1N	AL21
NC_UPHYAB_TMDPB_TX1P	AK20
NC_UPHYAB_TMDPB_TX2N	AH22
NC_UPHYAB_TMDPB_TX2P	AJ21
NC_UPHYAB_TMDPB_TX3N	AL23
NC_UPHYAB_TMDPB_TX3P	AK22
NC_TXOUT_U3P	AK24
NC_TXOUT_U3N	AJ23

EV_SP@Meso/Exo_S3

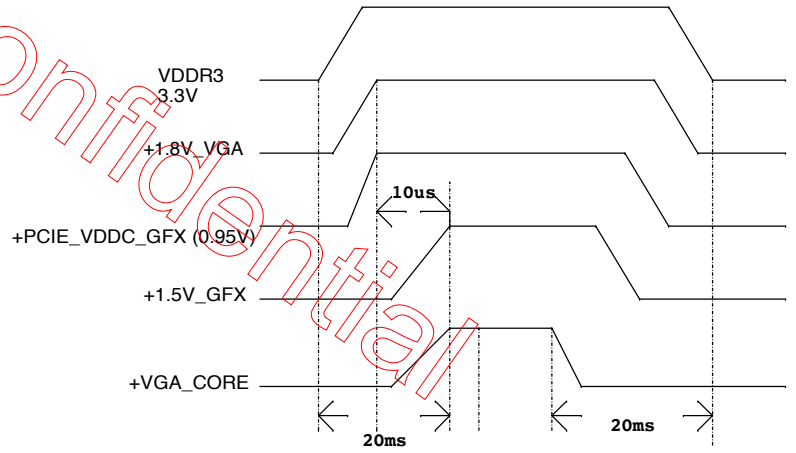
All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.

It is recommended that the 3.3-V rail ramp up first

The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 µs before VDDC, VDDCI, and VMEMIO start to ramp up.

For power down, reversing the ramp-up sequence is recommended.

Power Up/Down Sequence



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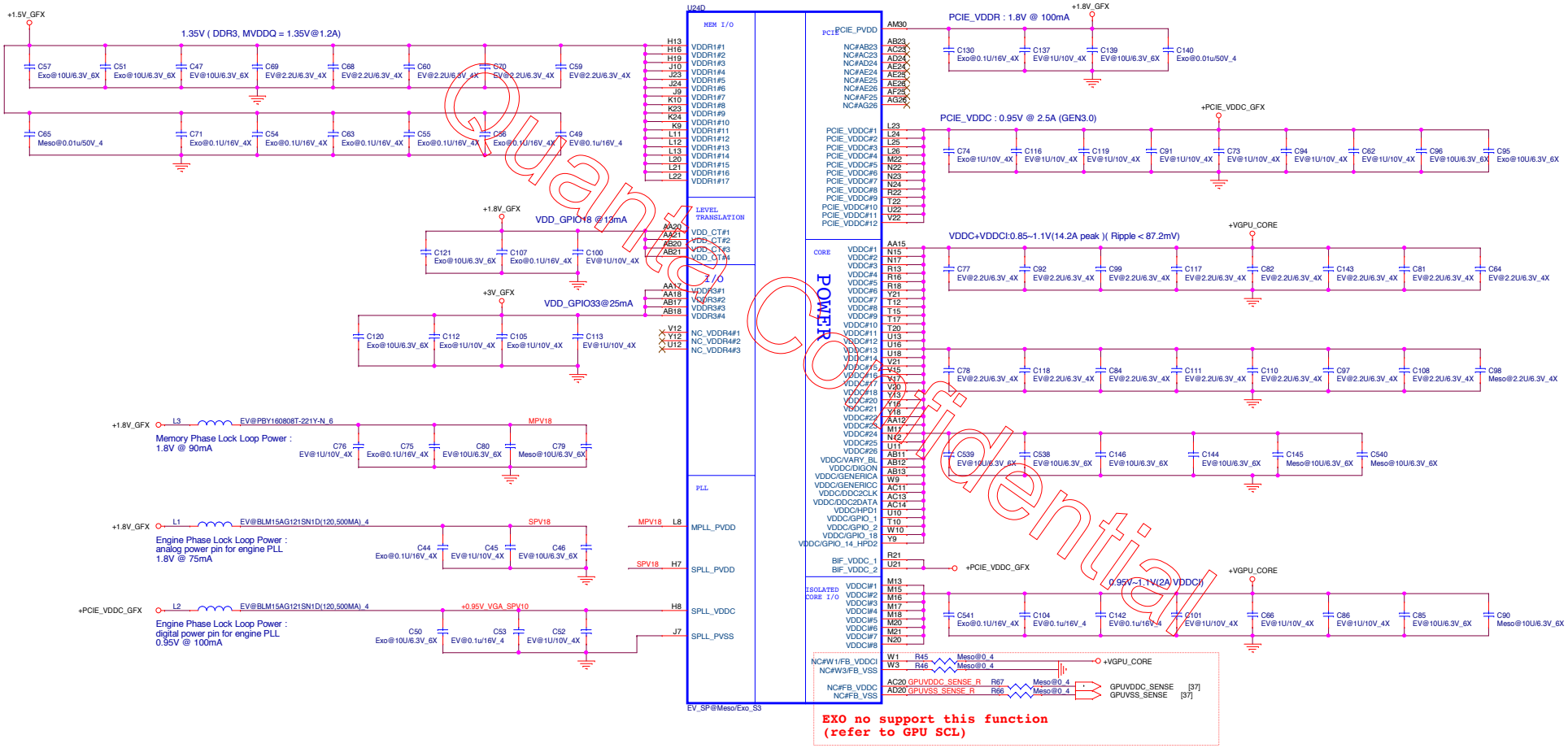
PROJECT : ZRZ

Size	Document Number	Rev
	Meso/Exo_S3_GND/LVDS/Strap(3/6)	1A

Date: Friday, March 06, 2015 Sheet 13 of 41

(VGA)



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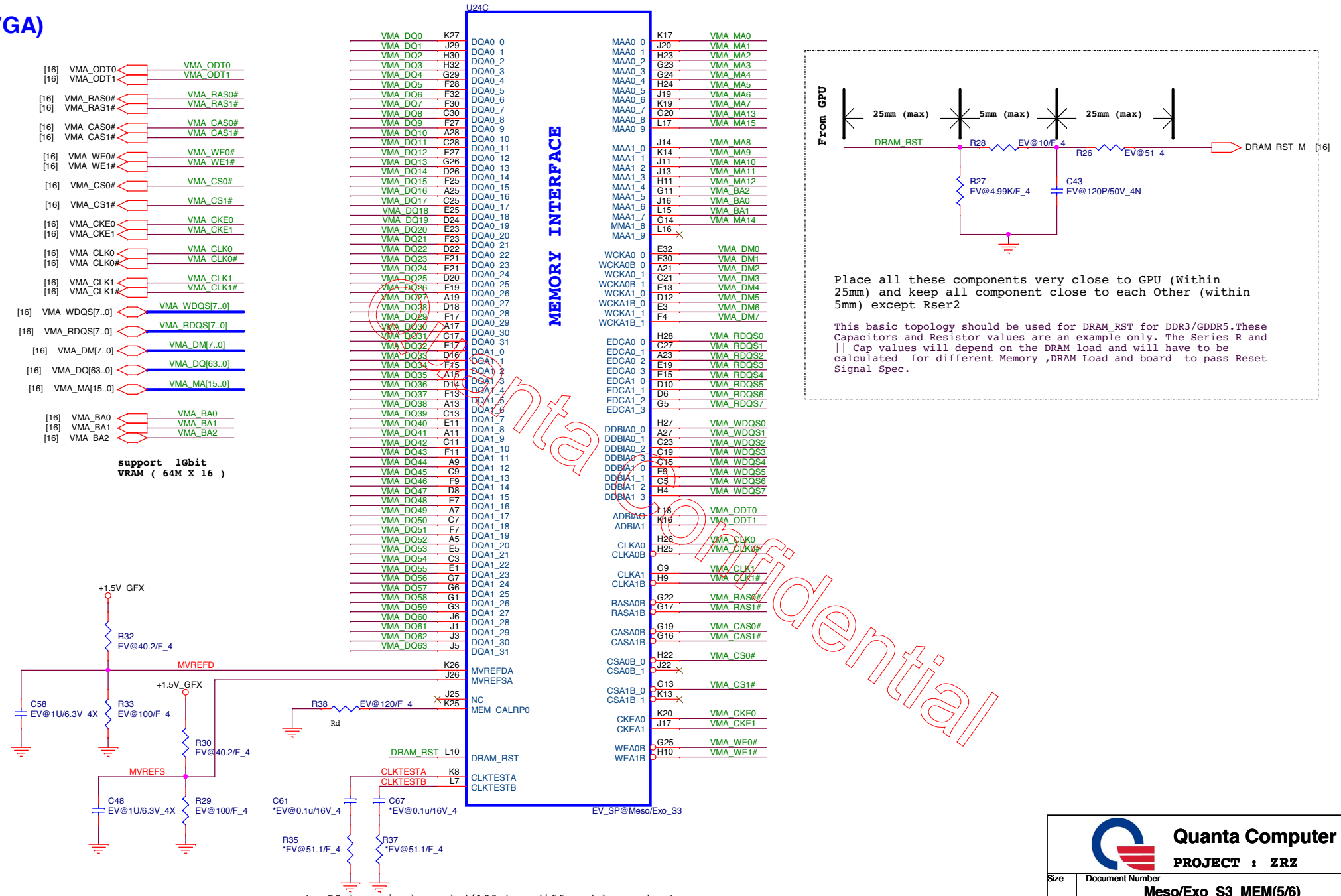
Quanta Computer Inc.		
PROJECT : ZRZ		
Size	Document Number: Meso/Exo_S3_Power(4/6)	Rev: 1A
Date: Wednesday, March 18, 2015	Sheet 14 of 41	

(VGA)



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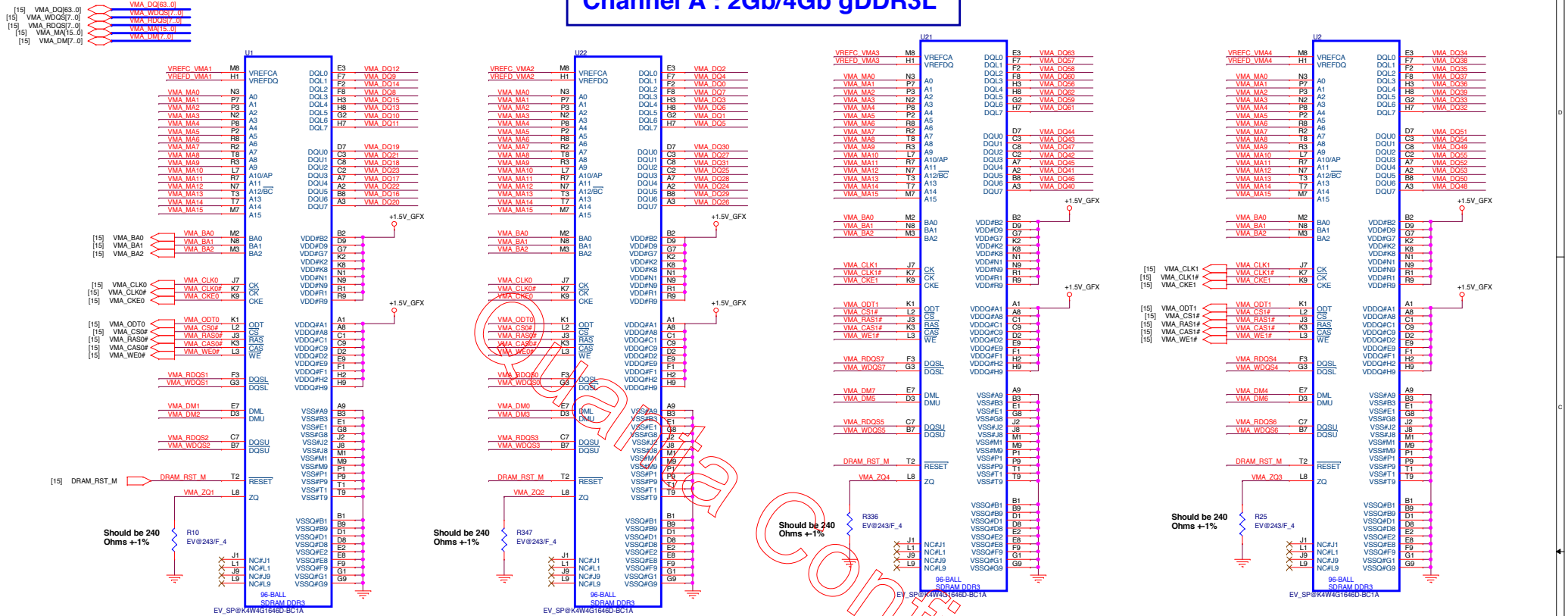
PROJECT : ZRZ

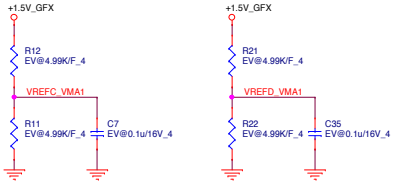
Size	Document Number	Rev
	Meso/Exo_S3_MEM(5/6)	1A
Date: Friday, March 06, 2015	Sheet 15 of 41	

(VGA)

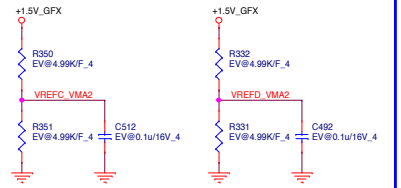
Channel A : 2Gb/4Gb gDDR3L



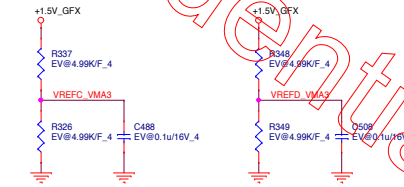
MEM Reference Voltage 1



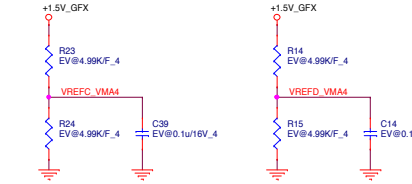
MEM Reference Voltage 2



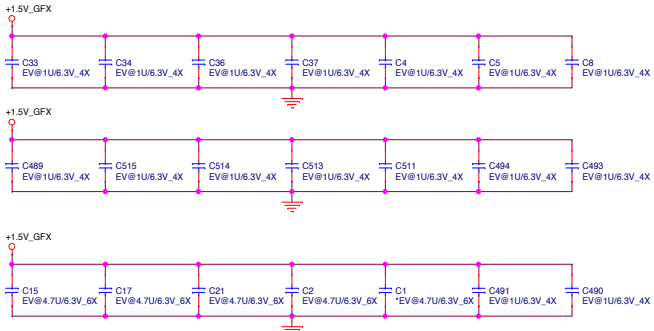
MEM Reference Voltage 3



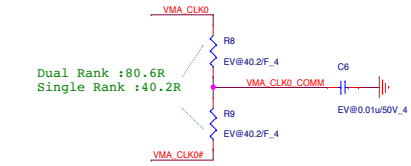
MEM Reference Voltage 4



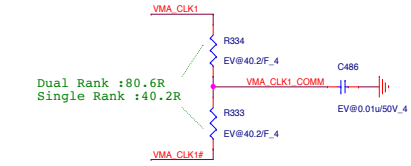
VRAM De-Coupling



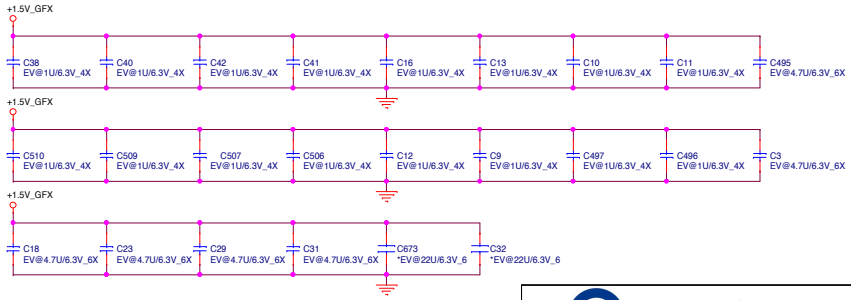
CLK-A0 Termination



CLK-A1 Termination



VRAM De-Coupling



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PROJECT : ZRZ

Size	Document Number	Rev
	Meso/Exo_S3_VRAM_DDR3 BGA(6/6)	1A
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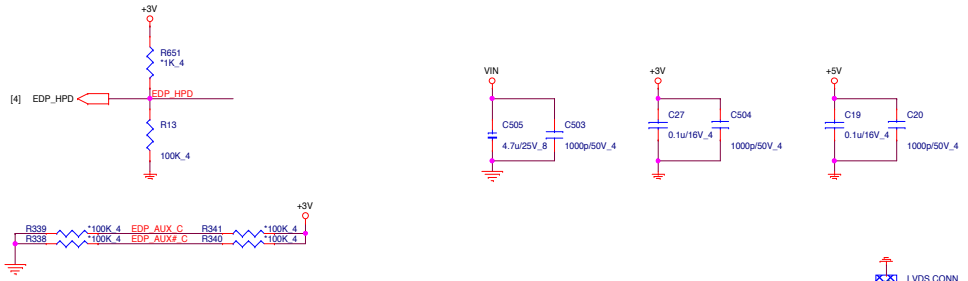
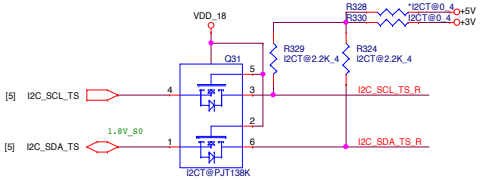
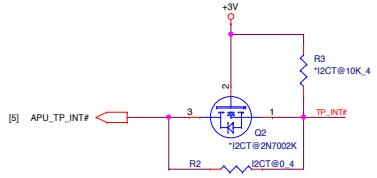
LCD (LDS)

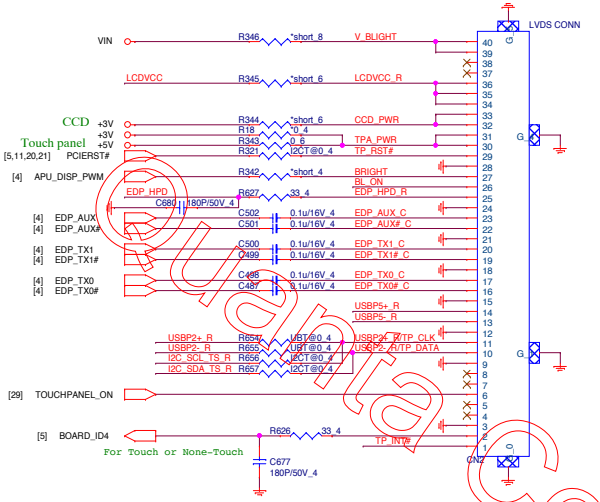


Front Camera (FCM)

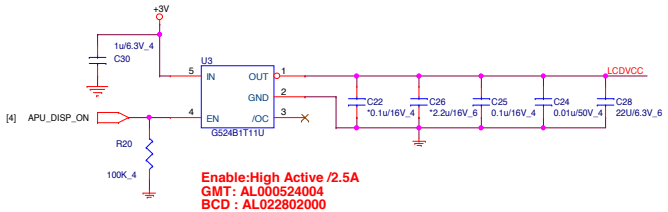
TOUCH (TSN)





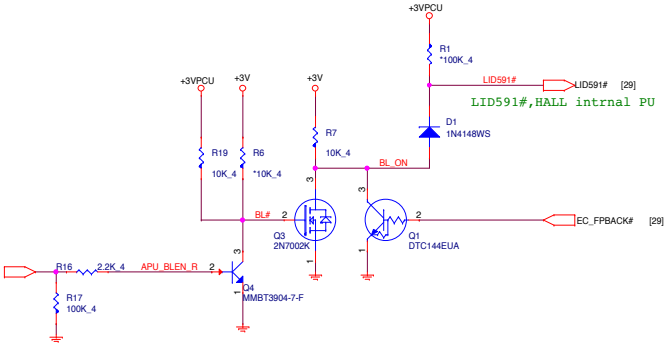


LCD Power (LDS)

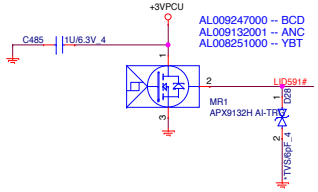


Enable:High Active /2.5A
GMT: AL000524004
BCD : AL022802000

Backlight Control (LDS)



Lid Switch (HSR)



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PROJECT : ZYV		
Size	Document Number: EDP/LID/CCD	Rev: D3B
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De-Mux (HDM)

3 Levels Input:
L: Low
H: High
M: VDD33/2, connect both pull-up and pull-down resistors

MODE = L: Control Switching Mode, HDMI ID disable
= H: Automatic Switching Mode, HDMI ID disable
= M: Automatic Switching Mode, HDMI ID enable

TMDS_PRE = L: no pre-emphasis
= H: 1.5dB pre-emphasis
= M: 3.0dB pre-emphasis

TMDS_RT = L: Standard open drain driver
= H: Open drain driver with termination resistors

TMDS_DDCBUF = L: DDC pass through
= H: DDC active buffer
= M: DDC pass through with 40 kohm pull up resistor

PEQ = L: default, LEQ, compensate channel loss up to 12dB @ HBR2
= H: HEQ, compensate channel loss up to 15dB @ HBR2
= M: LLEQ, compensate channel loss up to 5dB @ HBR2

DP_CFG1 = L: default, auto test disable & input offset cancellation enable
= H: auto test enable & input offset cancellation enable
= M: auto test disable & input offset cancellation disable

DP_CFG0 = L: default, automatic EQ enable & AUX interception enable
= H: automatic EQ disable & AUX interception enable
= M: automatic EQ disable & AUX interception disable, no pre-emphasis, 800mVpp swing

MUX_3V
R185 4.7K/J_4 MODE
R191 *4.7K/J_4 TMDS_PRE
R194 *4.7K/J_4 TMDS_RT
R180 *4.7K/J_4 TMDS_DDCBUF
R179 *4.7K/J_4 PEQ
R190 4.7K/J_4 SW
R184 4.7K/J_4
R192 *4.7K/J_4
R195 *4.7K/J_4
R182 *4.7K/J_4
R178 *4.7K/J_4
R636 *4.7K/J_4

HDMI switching to VGA need 100-400ms

MUX_3V
R200 *4.7K/J_4 DP_CFG1
R196 *4.7K/J_4 DP_CFG0
R201 *4.7K/J_4
R193 *4.7K/J_4

DP_AUXP_SCL [19]
DP_AUXN_SDA [19]
DP_AUXP_SCL R638 CZL@100K_4
DP_AUXN_SDA R639 CZL@100K_4
MUX_3V

For Control Switching:
SW = L: DP output is selected
SW = H: TMDS output is selected

For Automatic Switching:
SW = L: DP output has higher priority.
SW = H:TMDS output has higher priority.

+3V R203 *short_6 MUX_3V

+3V
R648 *10K_4
R649 *100K_4
[4] MUX_HPD

[4] MUX_TX0 C331 0.1U/16V/X7R_4 IN_D0P
[4] MUX_TX0# C330 0.1U/16V/X7R_4 IN_D0N
[4] MUX_TX1 C329 0.1U/16V/X7R_4 IN_D1P
[4] MUX_TX1# C328 0.1U/16V/X7R_4 IN_D1N
[4] MUX_TX2 C327 0.1U/16V/X7R_4 IN_D2P
[4] MUX_TX2# C326 0.1U/16V/X7R_4 IN_D2N
[4] MUX_TX3 C325 0.1U/16V/X7R_4 IN_D3P
[4] MUX_TX3# C324 0.1U/16V/X7R_4 IN_D3N
C334 2.2u/6.3V_4
C323 0.1u/16V_4 MUX_3V

C336 0.01u/50V_4

U13 PS8339B

1	CEXT	42	DP_CA_DET
2	TMDS_DDCBUF	41	VDD33
3	IN_D0p	40	DP_D0p
4	IN_D0n	39	DP_D0n
5	IN_HPD	38	I2C_CTL_EN
6	IN_D1p	37	DP_D1p
7	IN_D1n	36	DP_D1n
8	PEQ	35	GND
9	IN_D2p	34	DP_D2p
10	IN_D2n	33	DP_D2n
11	IN_CA_DET	32	DP_HPD
12	IN_D3P	31	DP_D3p
13	IN_D3n	30	DP_D3n
14	VDD33	29	DP_CFG1

DP_CA_DET R637 1M_4
MUX_3V C350 0.1u/16V_4
DP_D0P [19]
DP_D0N [19]
DP_D1P [19]
DP_D1N [19]
DP_HPD [19]
DP_CFG1

PS8339BQFN56GTR2-A1

PS8339B - Pin Control Mode

MUX_3V
R183 2.2K_4
R186 2.2K_4
R181 4.7K/F_4
Q19 BSS84
Q20 BSS84
Q18 2N7002K
IN_CA_DET

[4] MUX_AUX C338 0.1u/16V_4 IN_AUXP
[4] MUX_AUX# C340 0.1u/16V_4 IN_AUXN

C351 0.01u/50V_4
R198 4.99K/F_4

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HDMI(HDM)

EMI
TMDS_D2+ R576 *120/F_4 TMDS_D2-
TMDS_D1+ R567 *120/F_4 TMDS_D1-
TMDS_D0+ R564 *120/F_4 TMDS_D0-
TMDS_CLK+ R560 *120/F_4 TMDS_CLK-

*CM1225-04DE ESD4
*CM1225-04DE ESD3
GND_3/8

+5V
Q46 AP2802NTR-G1-01
BCD : AL002802002
DDS : AL002331000
C638 *220p/50V_4
D38 *EGA_4

TMDS_HPD R172 *short_4

HDMI_5V
R173 2.2K_4
R174 2.2K_4
D6 *EGA_4
D7 *EGA_4
D5 *EGA_4

CN10 HDMI connector

1	D2+	20	SHELL1
2	D2 Shield		
3	D2-		
4	D1+		
5	D1 Shield		
6	D1-		
7	D0+		
8	D0 Shield		
9	D0-	23	GND
10	CK+		
11	CK Shield	22	GND
12	CK-		
13	CE Remote		
14	NC		
15	DDC CLK		
16	DDC DATA		
17	GND		
18	+5V		
19	HP DET	21	SHELL2

TMDS_D2+ TMDS_D2- TMDS_D1+ TMDS_D1- TMDS_D0+ TMDS_D0- TMDS_CLK+ TMDS_CLK- TMDS_SCL TMDS_SDA HDMI_5V TMDS_HPD_R

Quanta Computer Inc.
PROJECT : ZRZ

Size	Document Number	Rev
	De-Mux (PS8339B)/HDMI	1A
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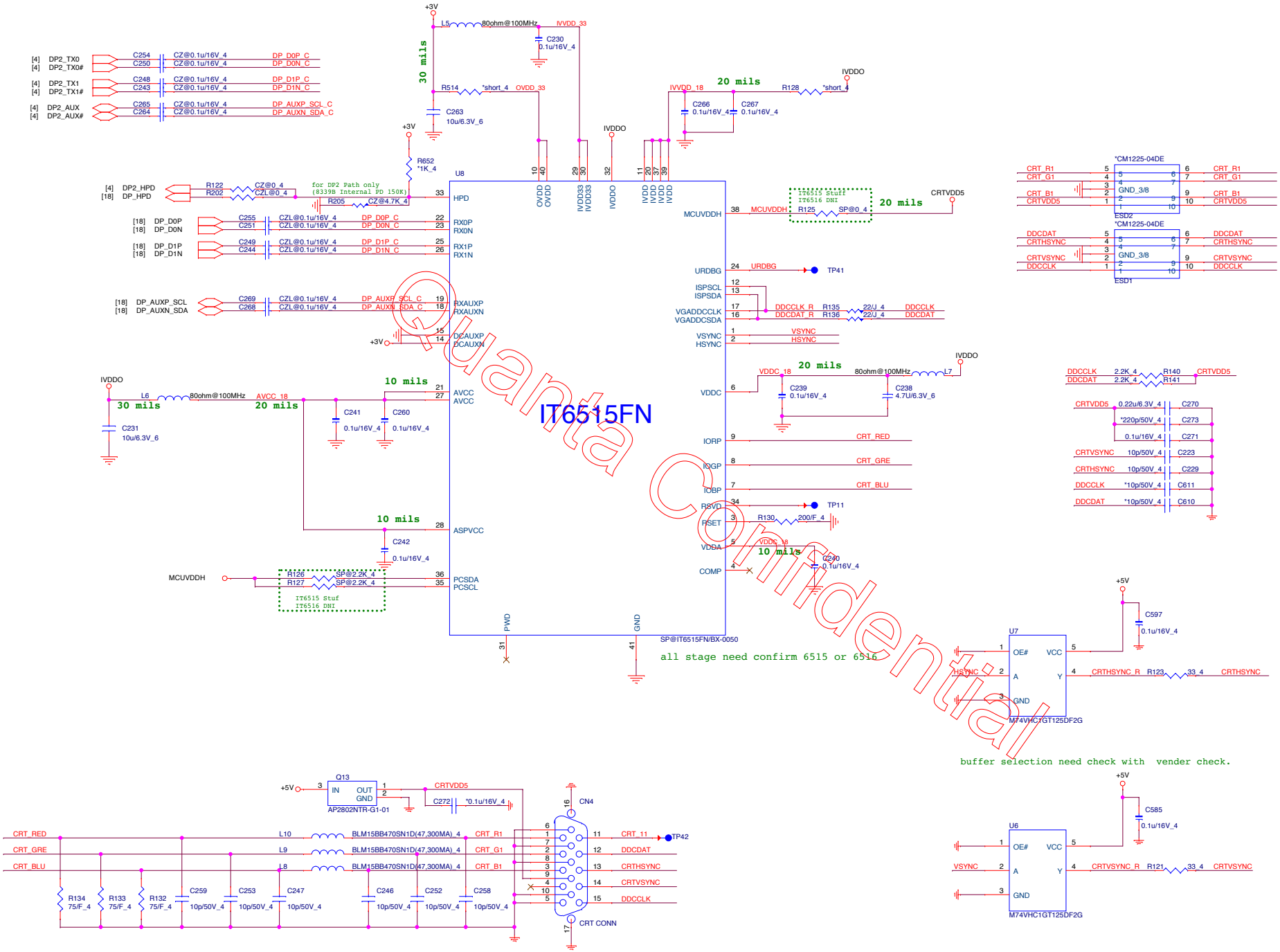
DP TO VGA (CRT)


U8
IT6515FN
SP@IT6515FN/BX-0050
all stage need confirm 6515 or 6516
buffer selection need check with vender check.
U7
U6
M74VHC1GT125DF2G
CN4
CRT CONN
Q13
AP2802NTR-G1-01
ESD1
ESD2
*CM1225-04DE
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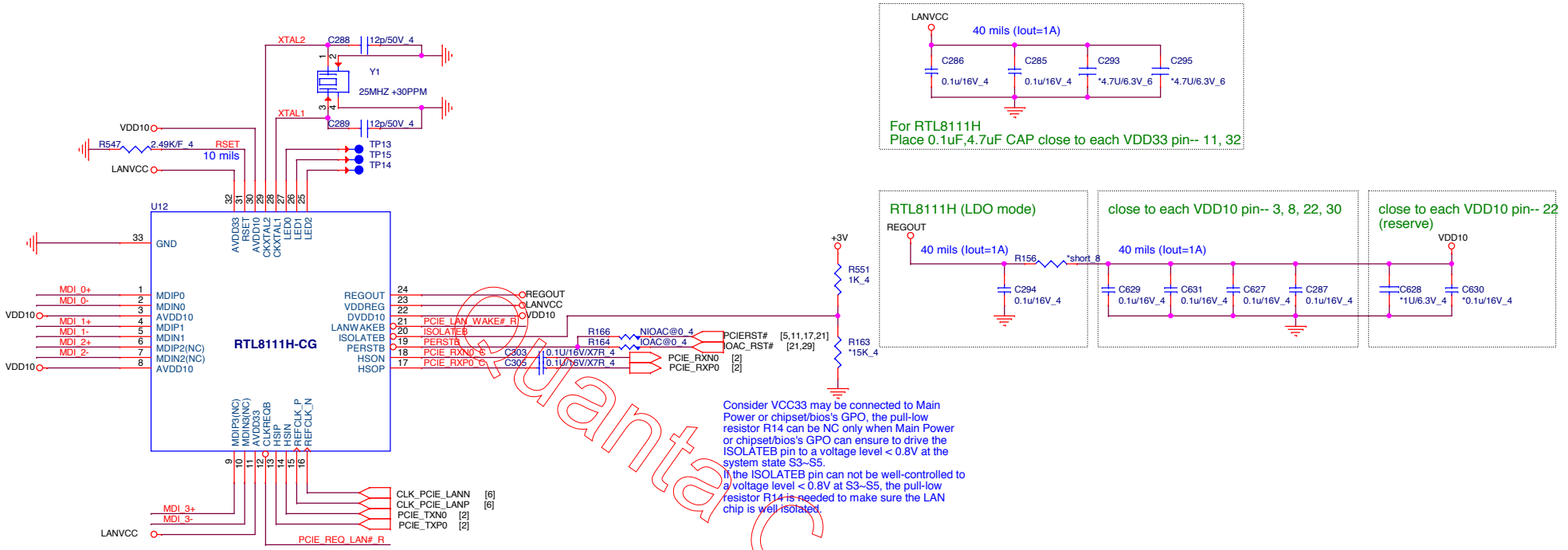
Giga LAN (LAN)



Consider VCC33 may be connected to Main Power or chipset/bios's GPO, the pull-low resistor R14 can be NC only when Main Power or chipset/bios's GPO can ensure to drive the ISOLATEB pin to a voltage level < 0.8V at the system state S3~S5.
If the ISOLATEB pin can not be well-controlled to a voltage level < 0.8V at S3~S5, the pull-low resistor R14 is needed to make sure the LAN chip is well isolated.

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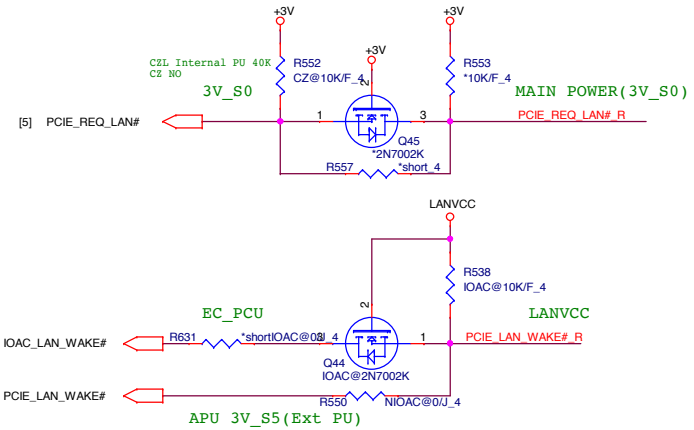
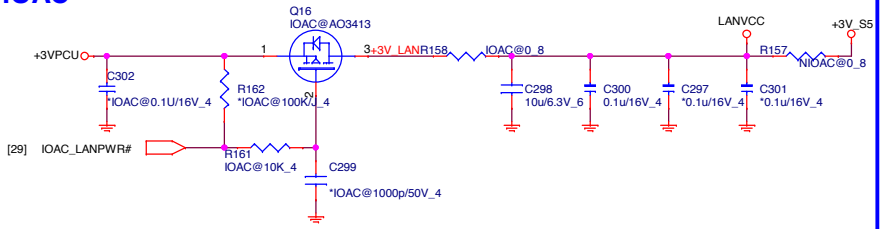
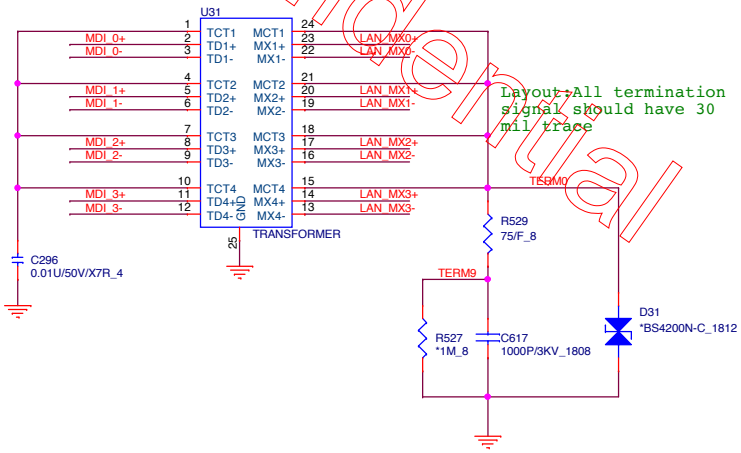
Leakage circuit



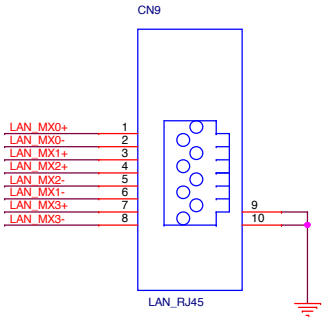
IOAC



Tramsformer



RJ45 Connector



Quanta Computer Inc.		
PROJECT : ZRZ		
Size	Document Number: LAN(RTL8111H)	Rev: 1A
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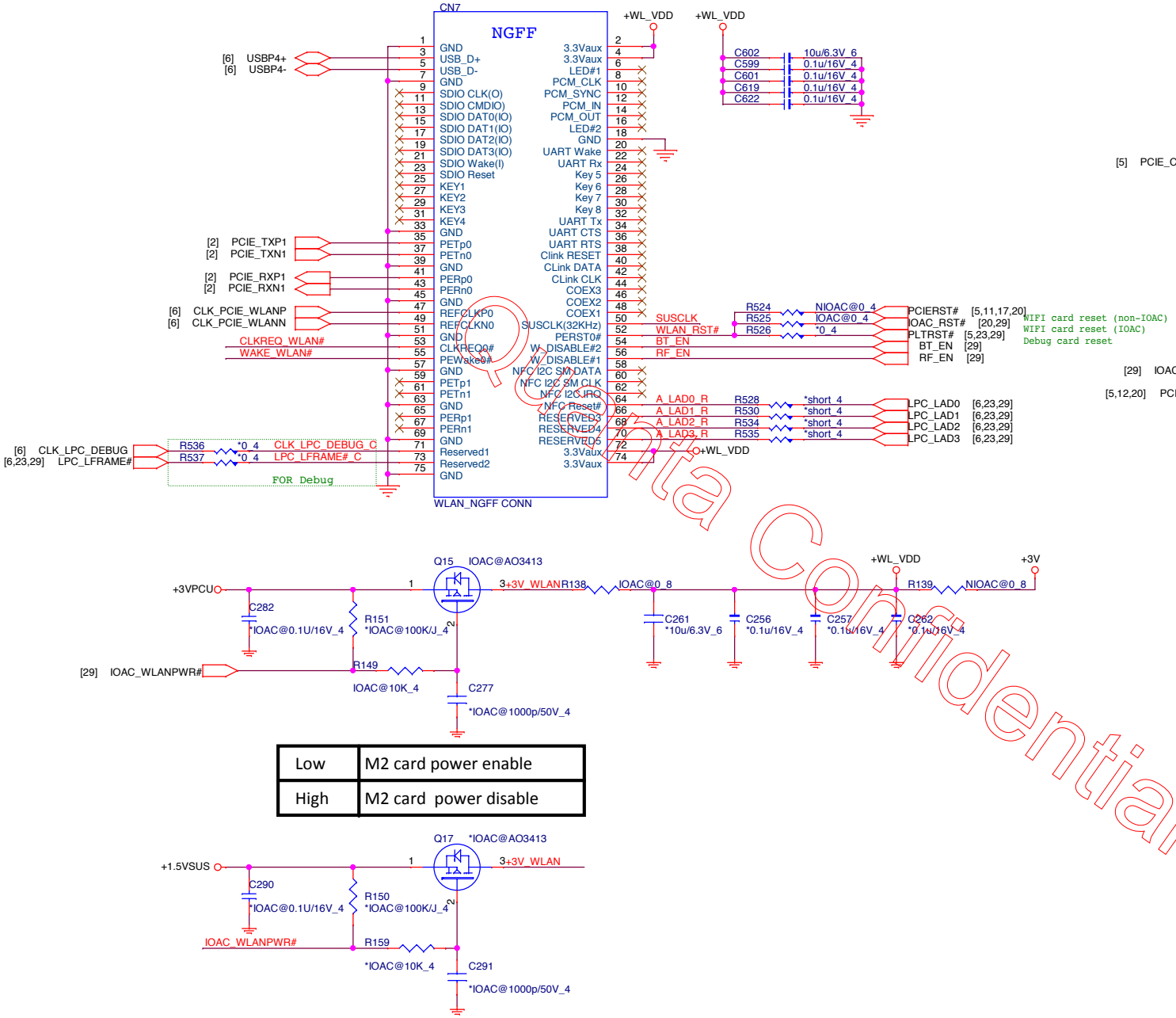
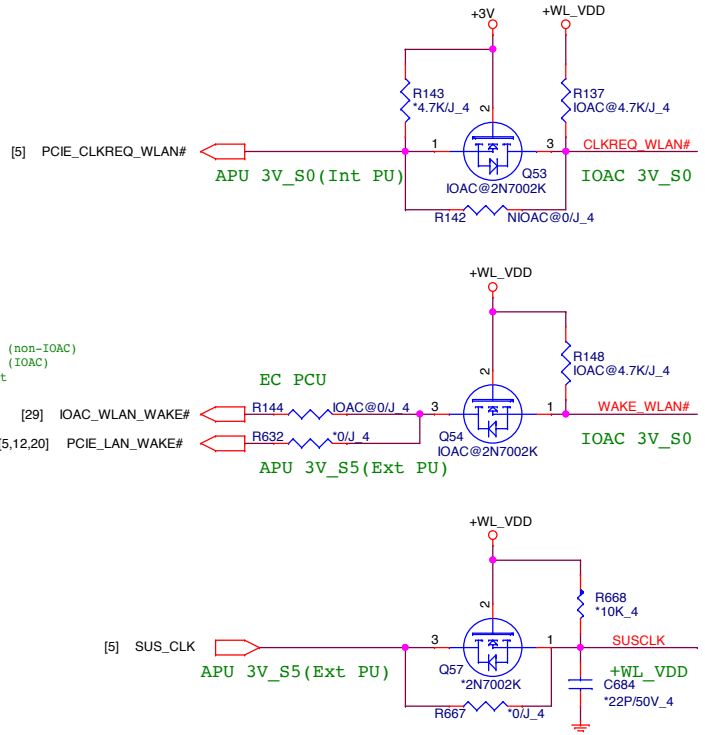
NGFF_M2 WiFi & BT (NGF)



Low	M2 card power enable
High	M2 card power disable

Leakage circuit



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PROJECT : ZRZ

Size	Document Number	Rev
	NGFF(WiFi&BT combo)	1A
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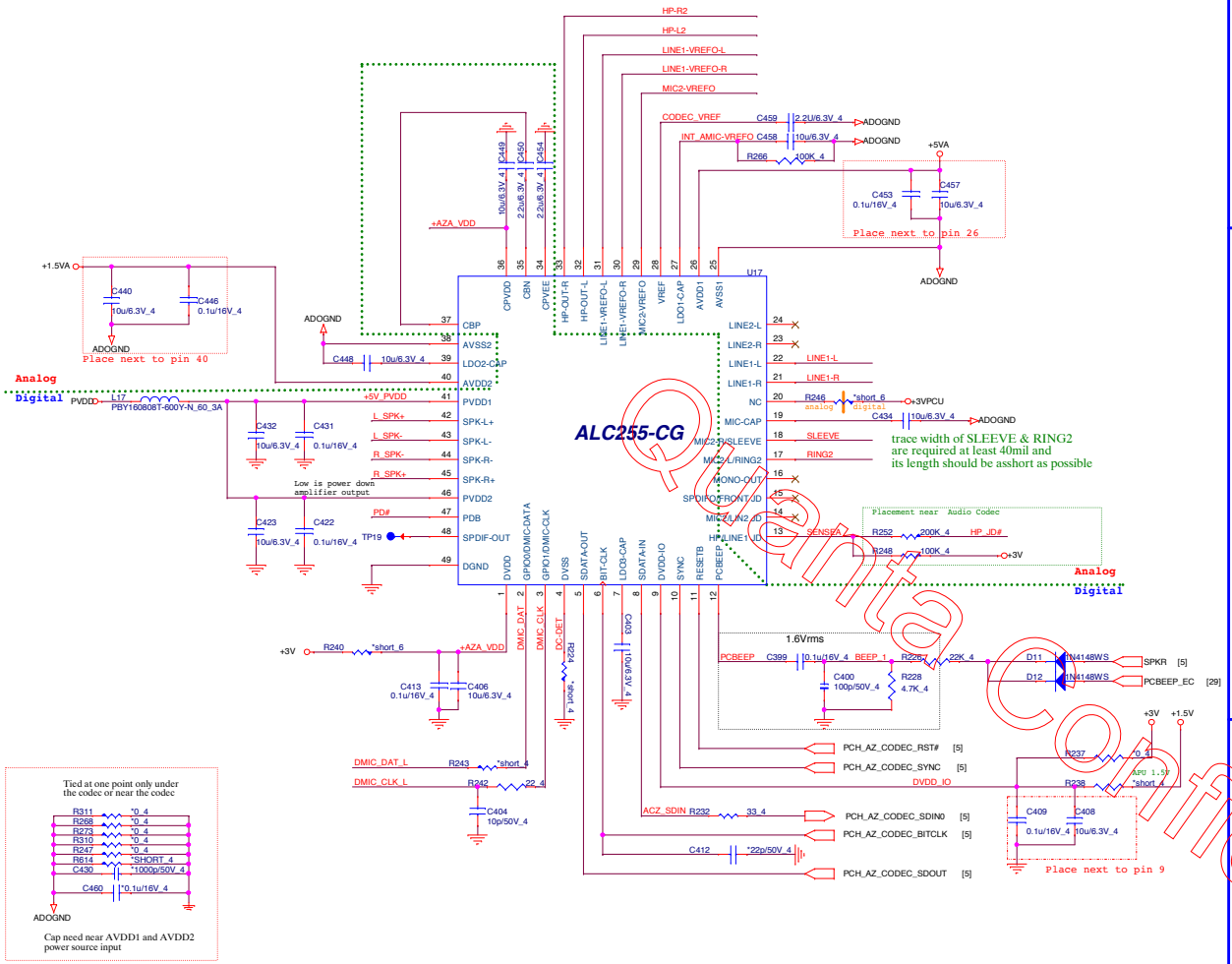
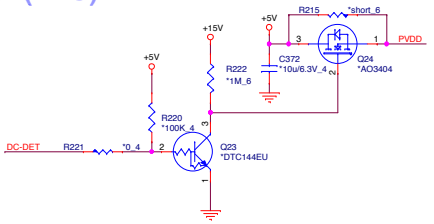
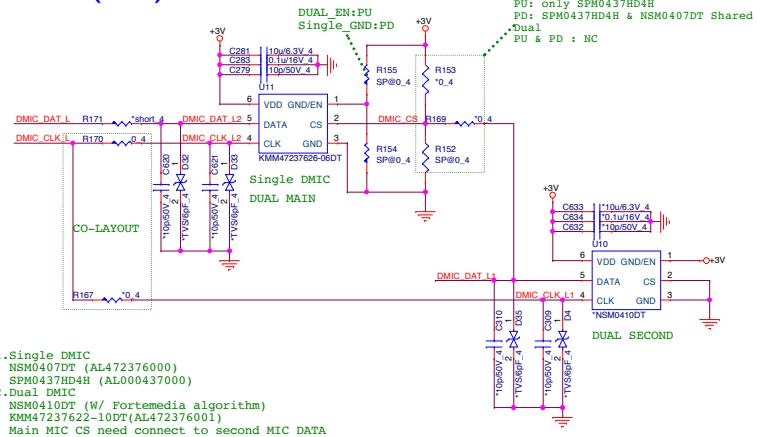
Codec(ADO)



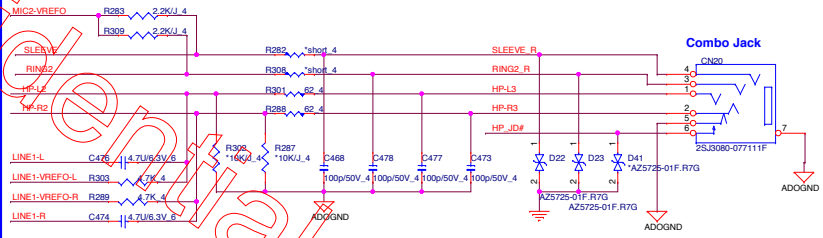
DC-DET circuit(ADO)



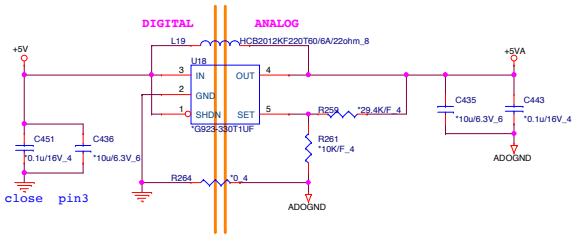
D-Mic (MIC)



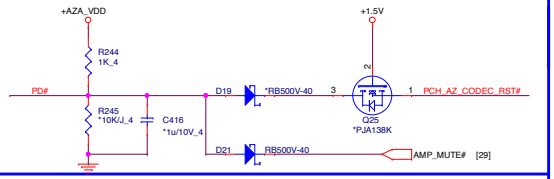
HEADPHONE/MIC/LINE combo (ADO)



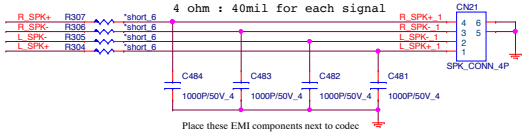
Codec PWR 5V(ADO)



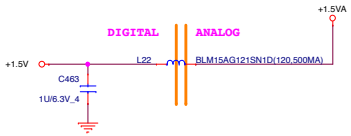
Mute(ADO)



Internal Speaker



Codec PWR 1.5V(ADO)



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Quanta Computer Inc.		
PROJECT : ZRZ		
Size	Document Number	Rev
	Audio Codec(AL255) / HP / SPK / DMIC	1A
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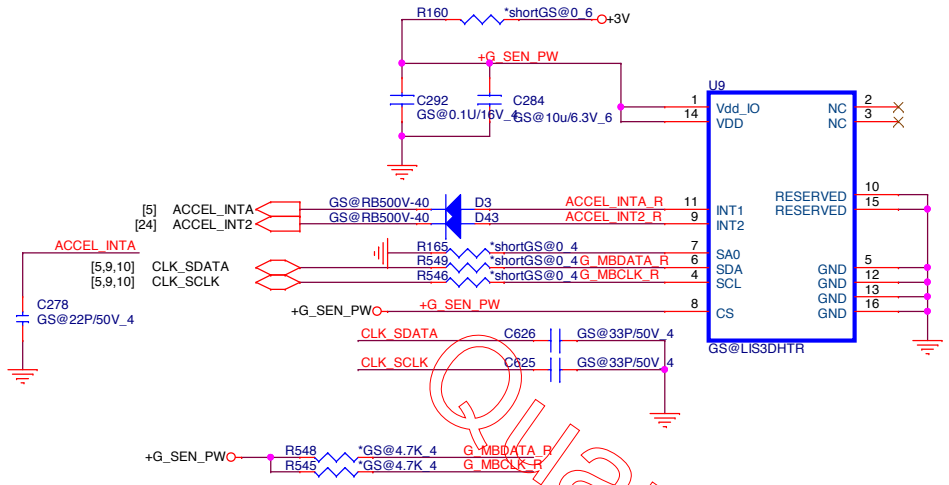
G-sensor (H3D)



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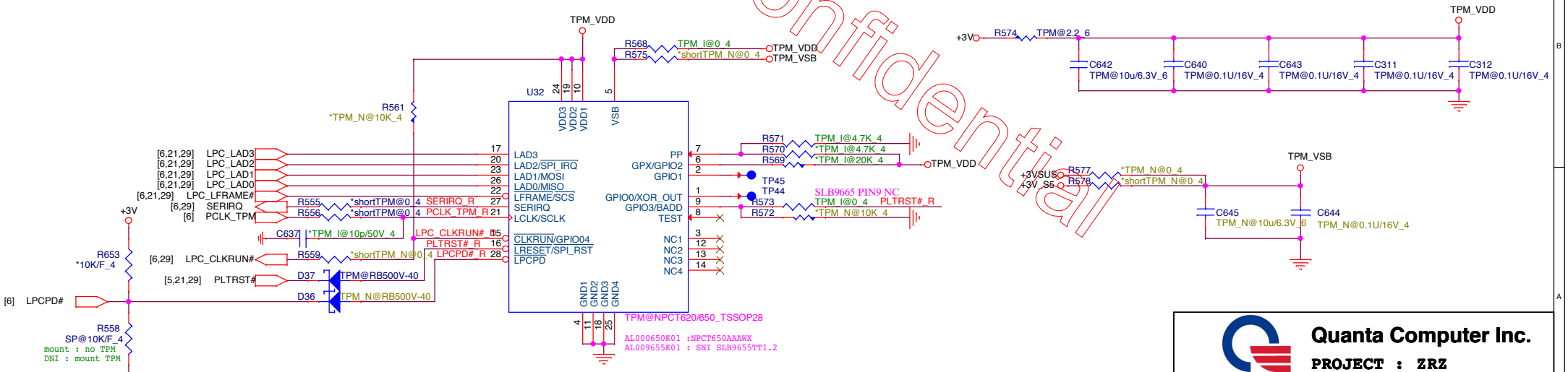
TPM (TPM)



Quanta Computer Inc.		
PROJECT : ZRZ		
Size	Document Number	Rev
	TPM (NPCT650)	1A
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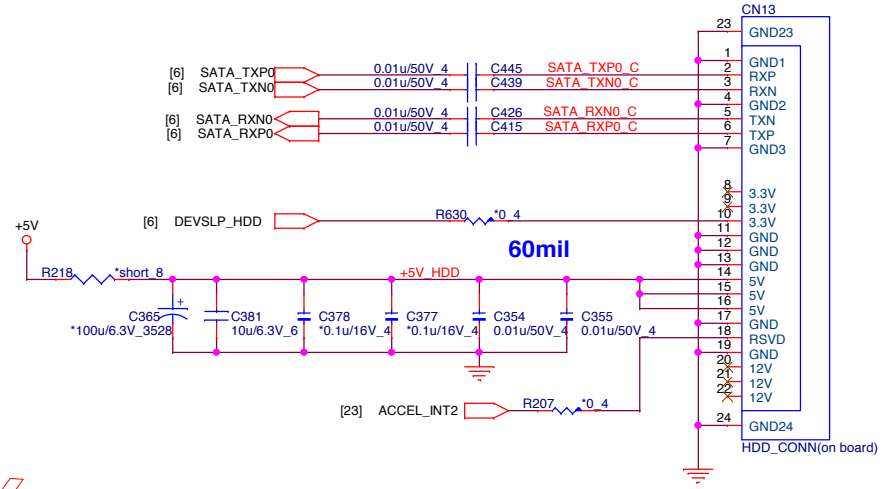
SATA HDD (HDD)



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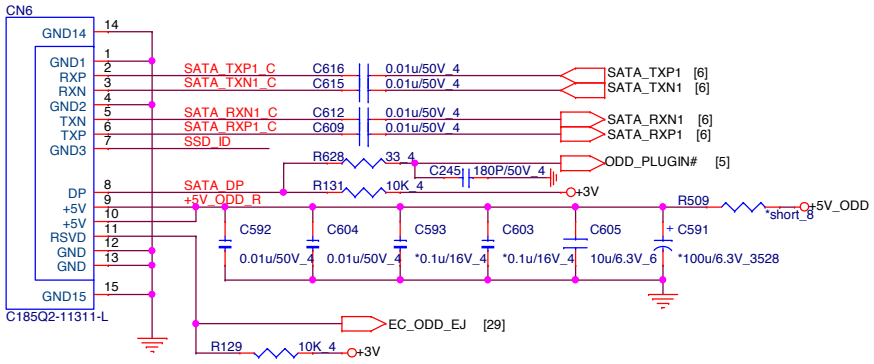
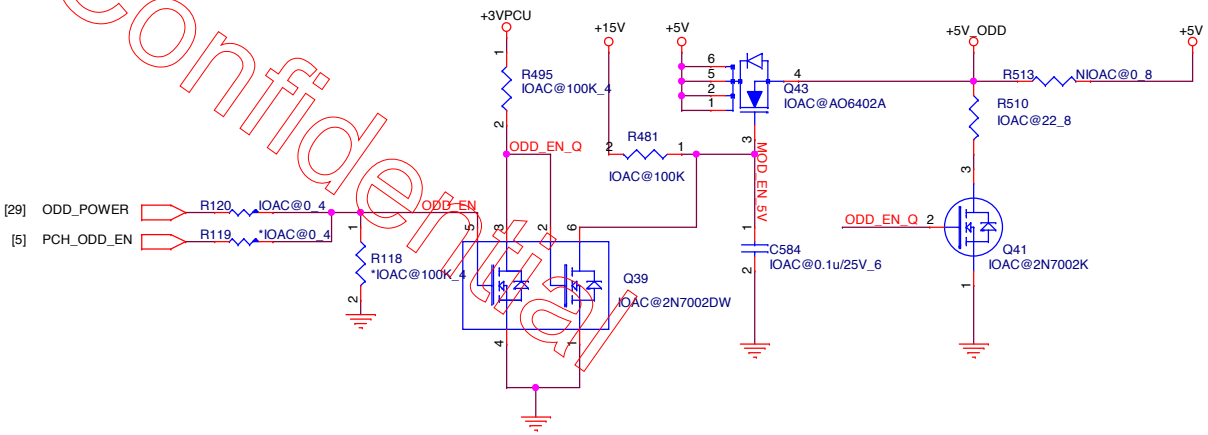
SATA ODD (ODD)



IOAC power



Quanta Computer Inc.		
PROJECT : ZRZ		
Size	Document Number	Rev
	SATA HDD / ODD	1A
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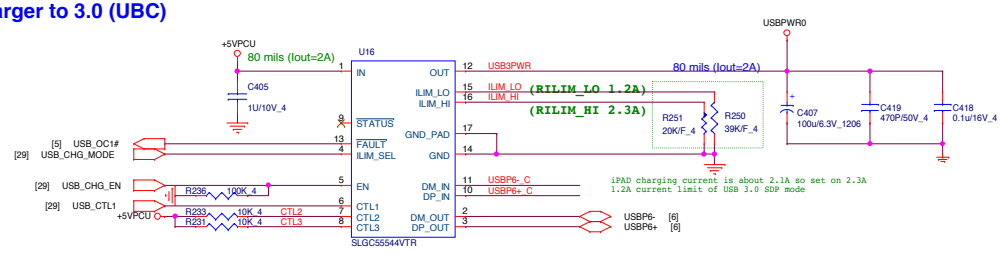
USB Charger to 3.0 (UBC)



	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

$$IOS_typ(mA) = 50{,}250/\{RILIM_XX(K\Omega)+0.1\}$$

GMT:AL003703000(G3703)_X
TI:AL002544001(TPS2544)
Silergy:AL055544000(SLGC55544VTR)

USB 3.0 Connector (UB3)

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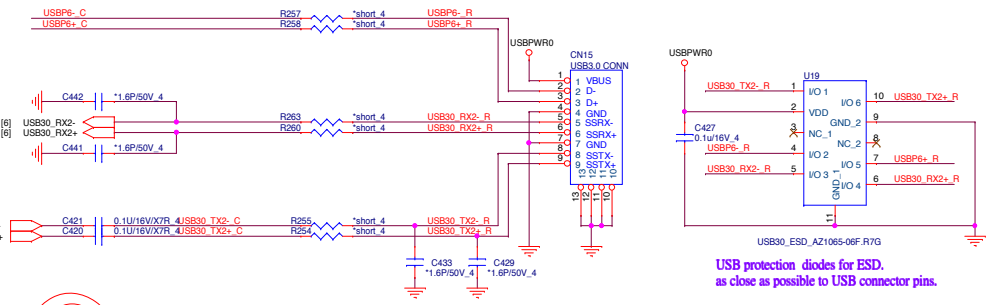
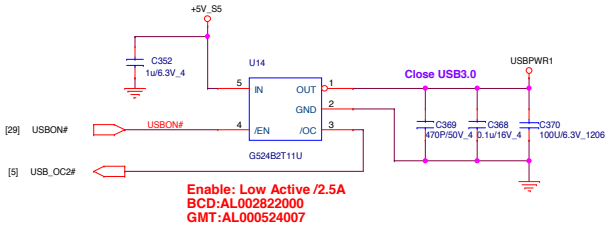
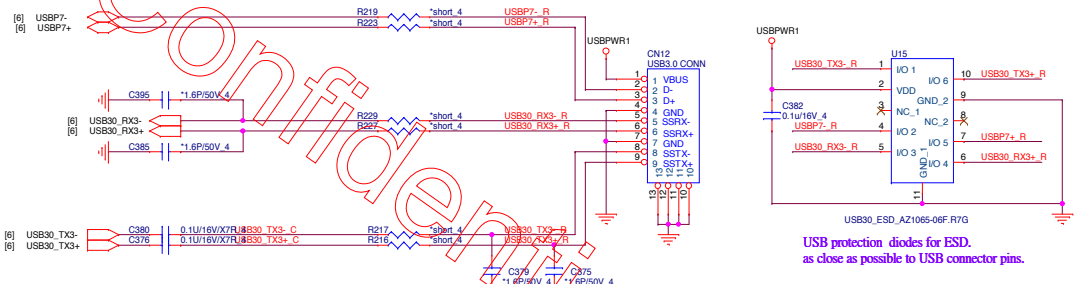
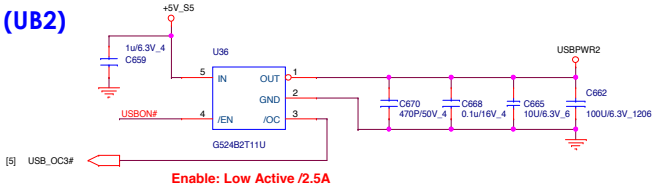
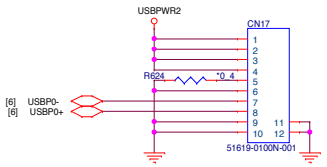




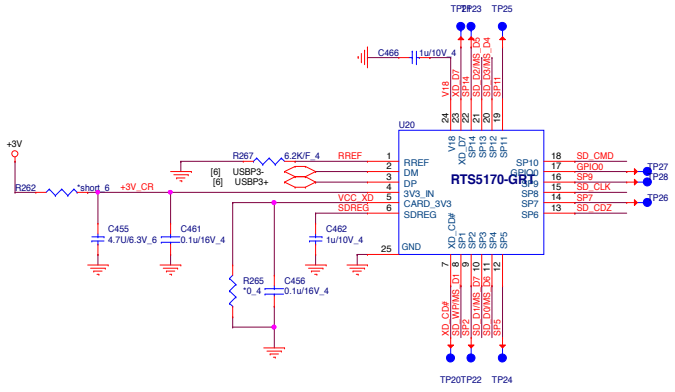


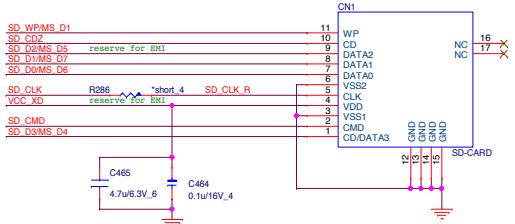
USB2.0 DB (UB2)





Card Reader (CRD)





Quanta Computer Inc.
PROJECT : ZRZ

Size	Document Number	Rev
	USB3/Charger/CR/USB2 DB	1A
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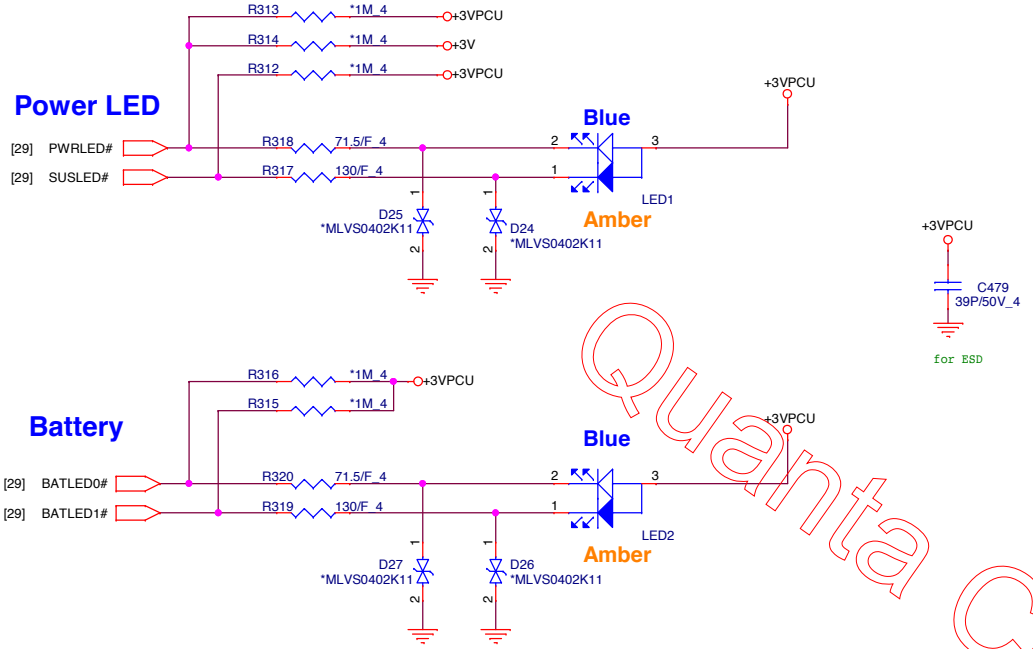
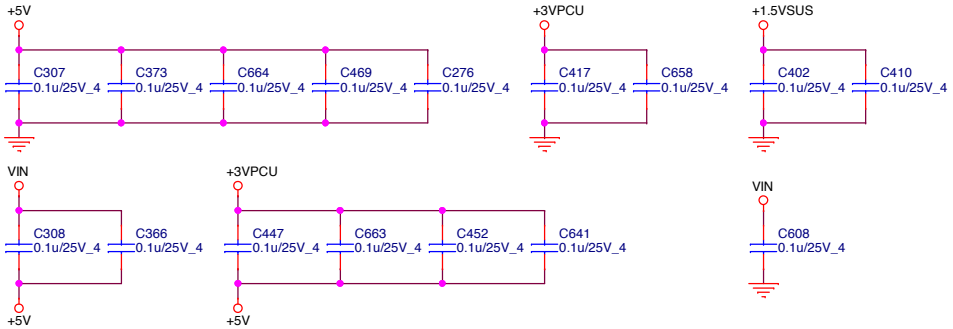
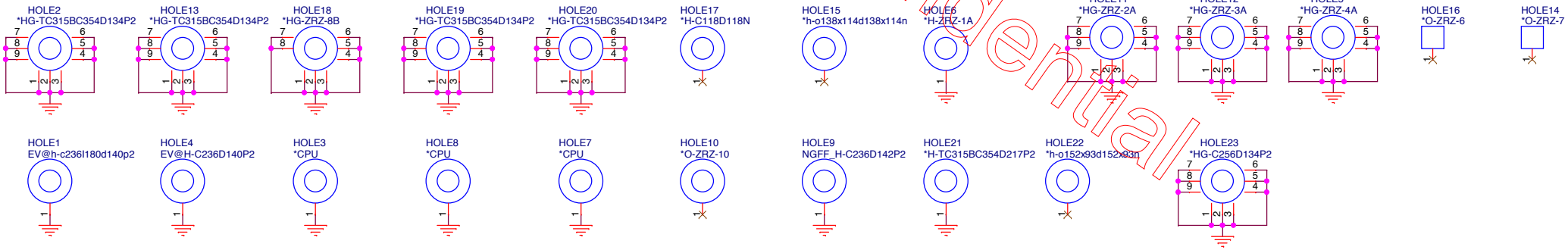
LED(UIF)

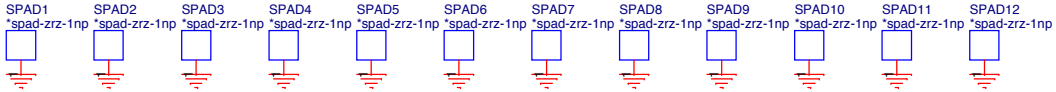


Stich cap



HOLE(OTH)





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PROJECT : ZRZ

Size	Document Number	Rev
	LED/HOLE/EMI	1A
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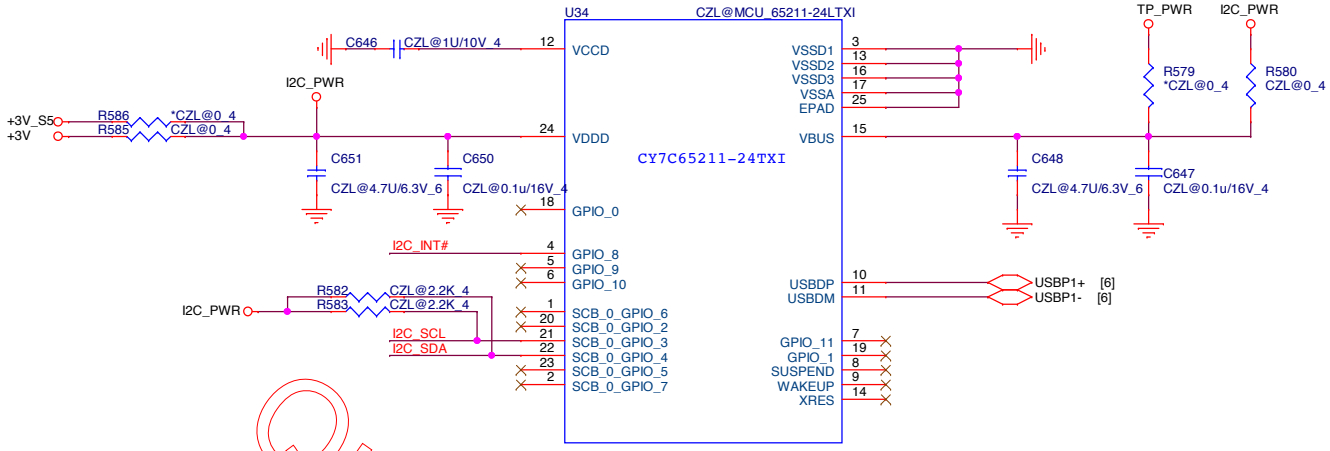
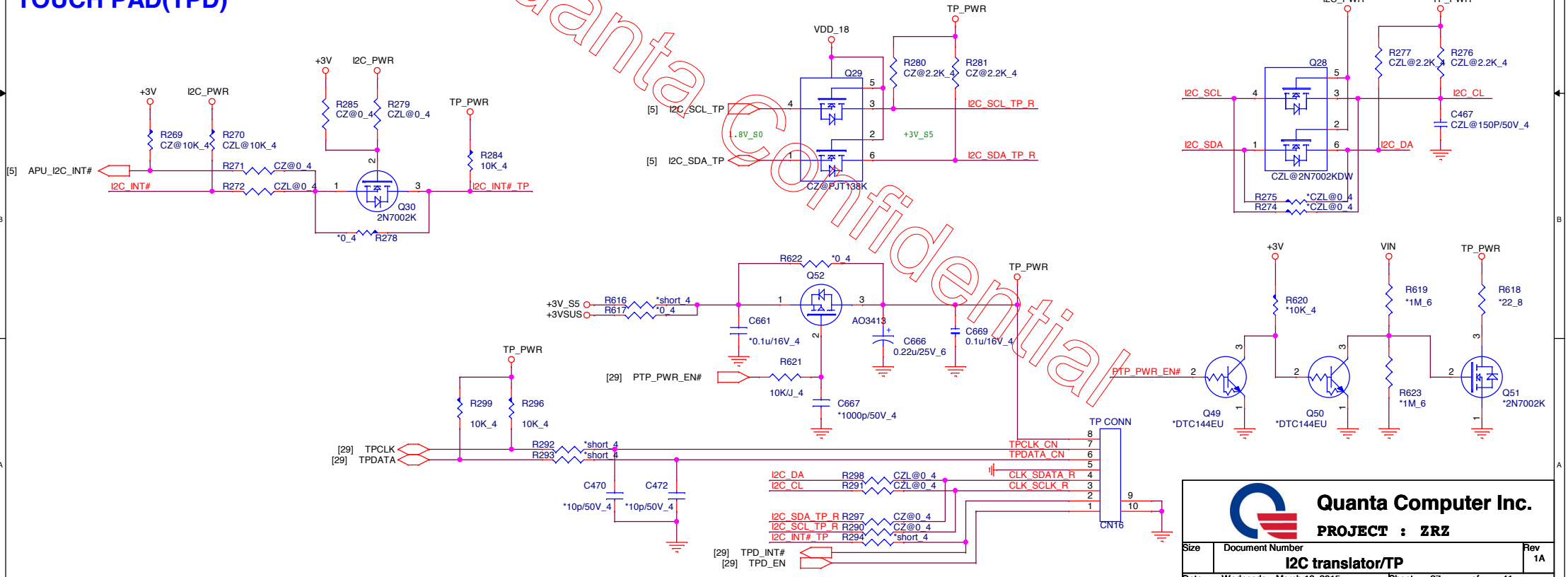
I2C translator (TPD)



TOUCH PAD(TPD)



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Quanta Computer Inc. PROJECT : ZRZ		
Size	Document Number: I2C translator/TP	Rev: 1A
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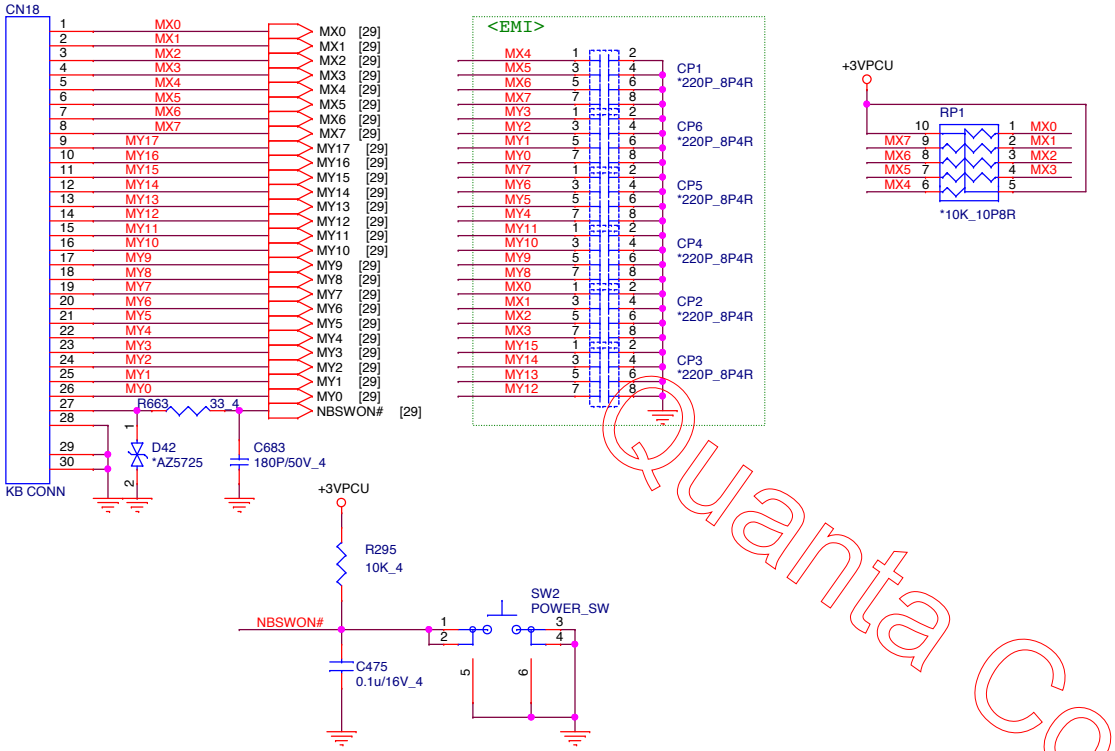
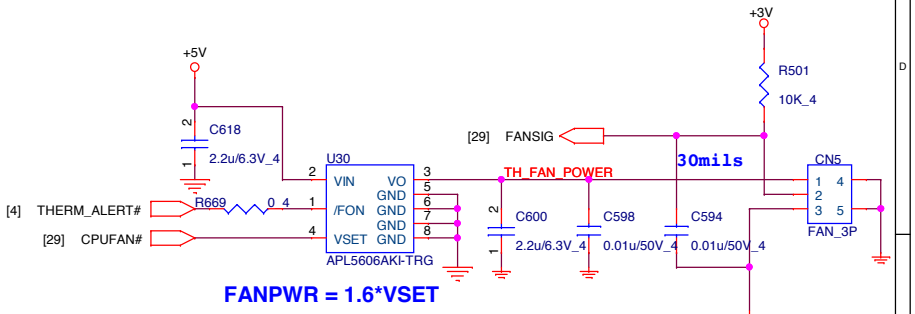
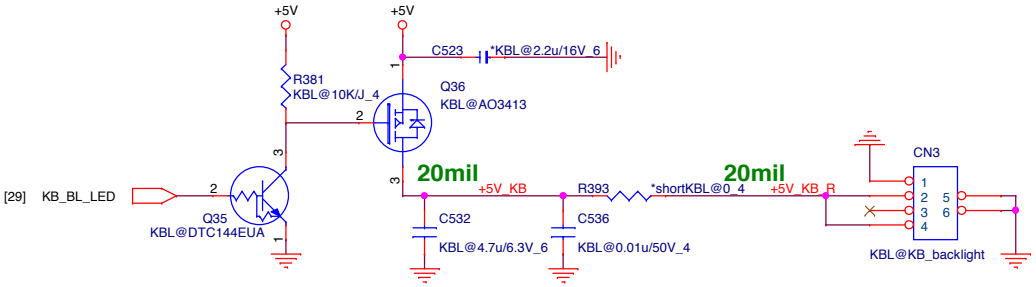
KEYBOARD (KBC)



CPU FAN CTRL(THM)



KB_BL LED (KBL)



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Quanta Computer Inc.

PROJECT : ZRZ

Size	Document Number	Rev
	KB/FAN	1A
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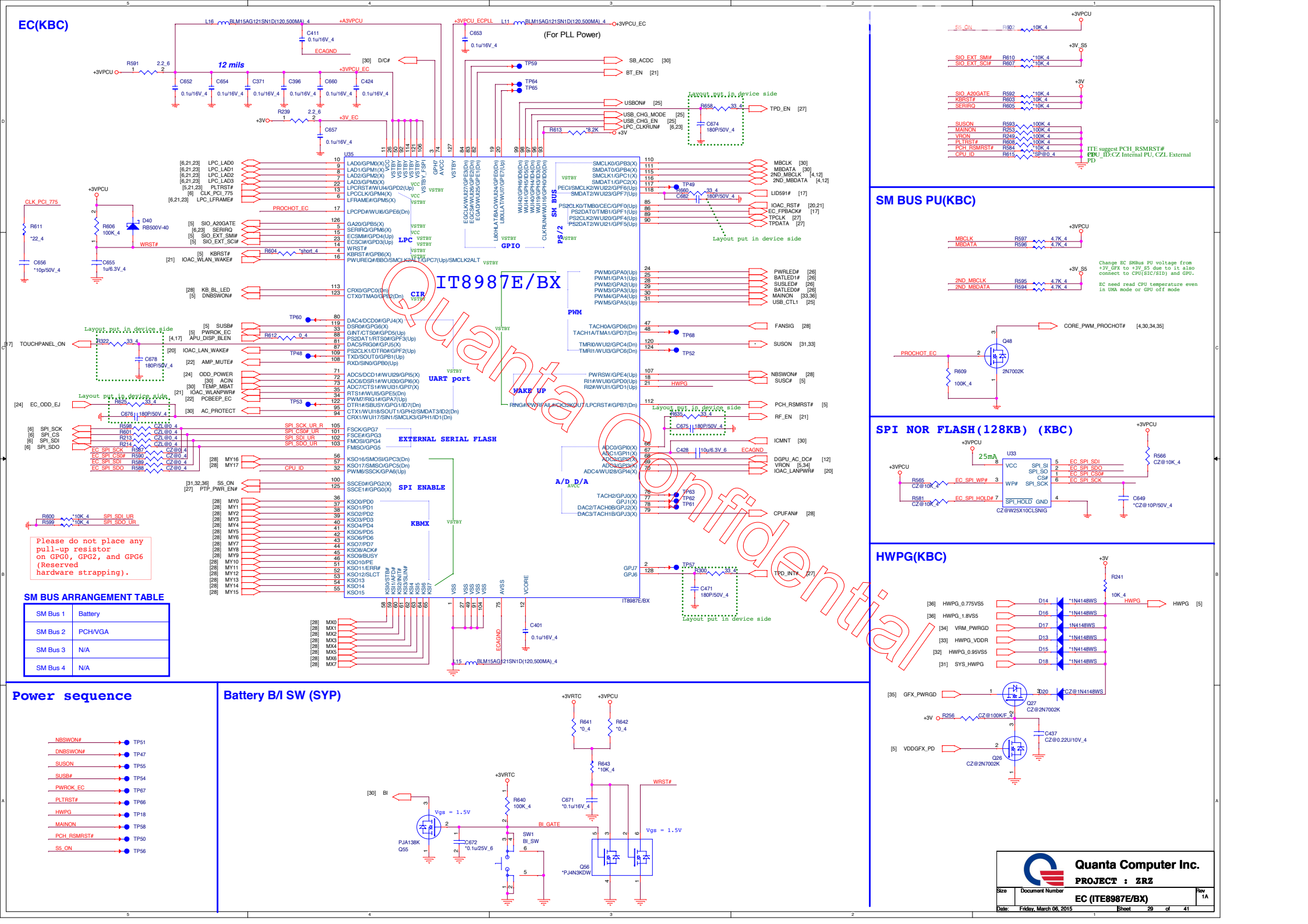
EC(KBC)
IT8987E/BX
SM BUS PU(KBC)
SPI NOR FLASH(128KB) (KBC)
HWPG(KBC)
SM BUS ARRANGEMENT TABLE
SM Bus 1 Battery
SM Bus 2 PCH/VGA
SM Bus 3 N/A
SM Bus 4 N/A
Please do not place any pull-up resistor on GPG0, GPG2, and GPG6 (Reserved hardware strapping).
Power sequence
Battery B/I SW (SYP)
Quanta Computer Inc.
PROJECT : ZRZ
EC (ITE8987E/BX)
Friday, March 06, 2015
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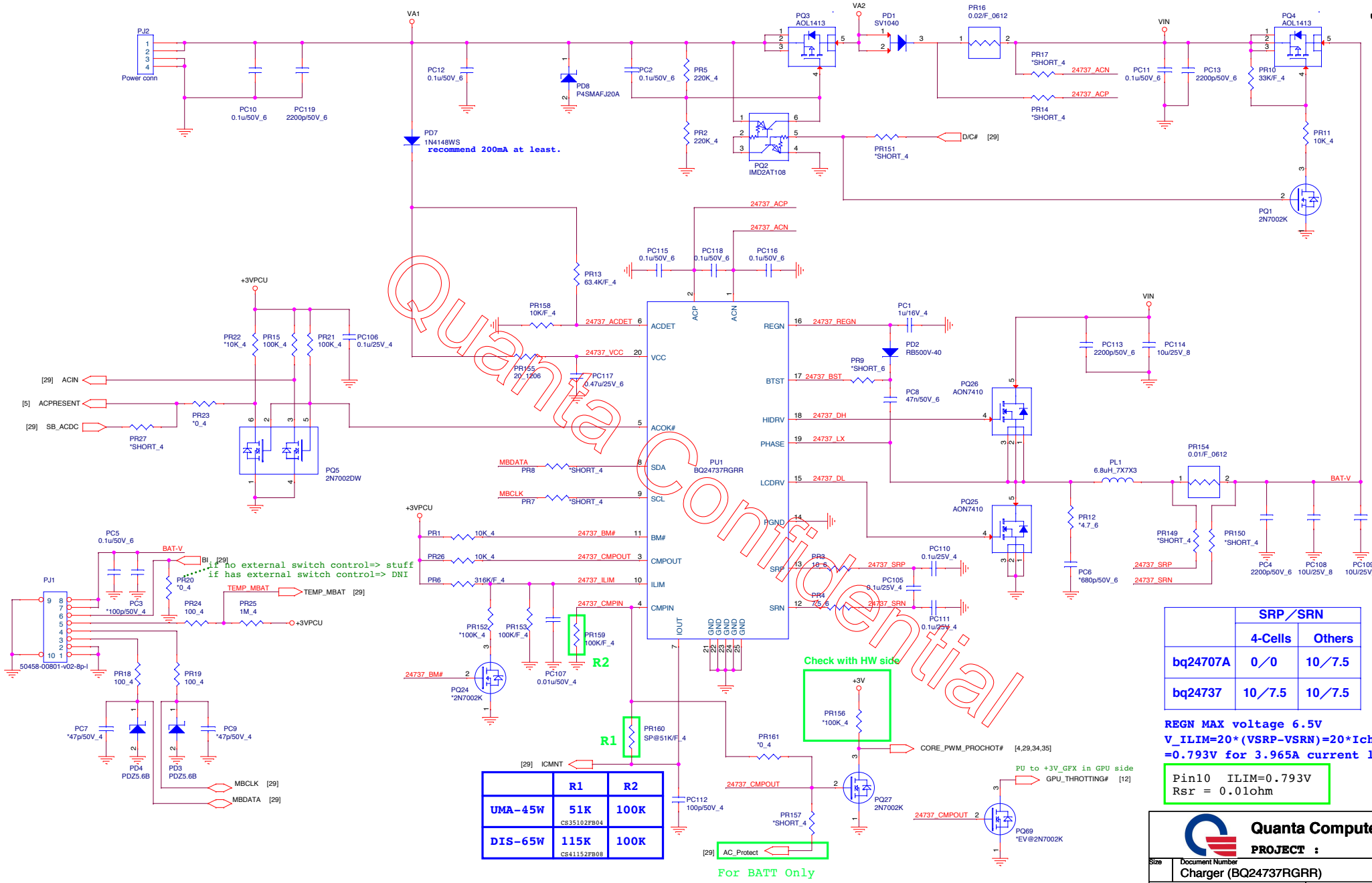

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	SRP/SRN	
	4-Cells	Others
bq24707A	0/0	10/7.5
bq24737	10/7.5	10/7.5

	R1	R2
UMA-45W	51K CS35102FB04	100K
DIS-65W	115K CS41152FB08	100K

REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit

Pin10 ILIM=0.793V
Rsr = 0.01ohm

Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
	Charger (BQ24737RGRR)	1A

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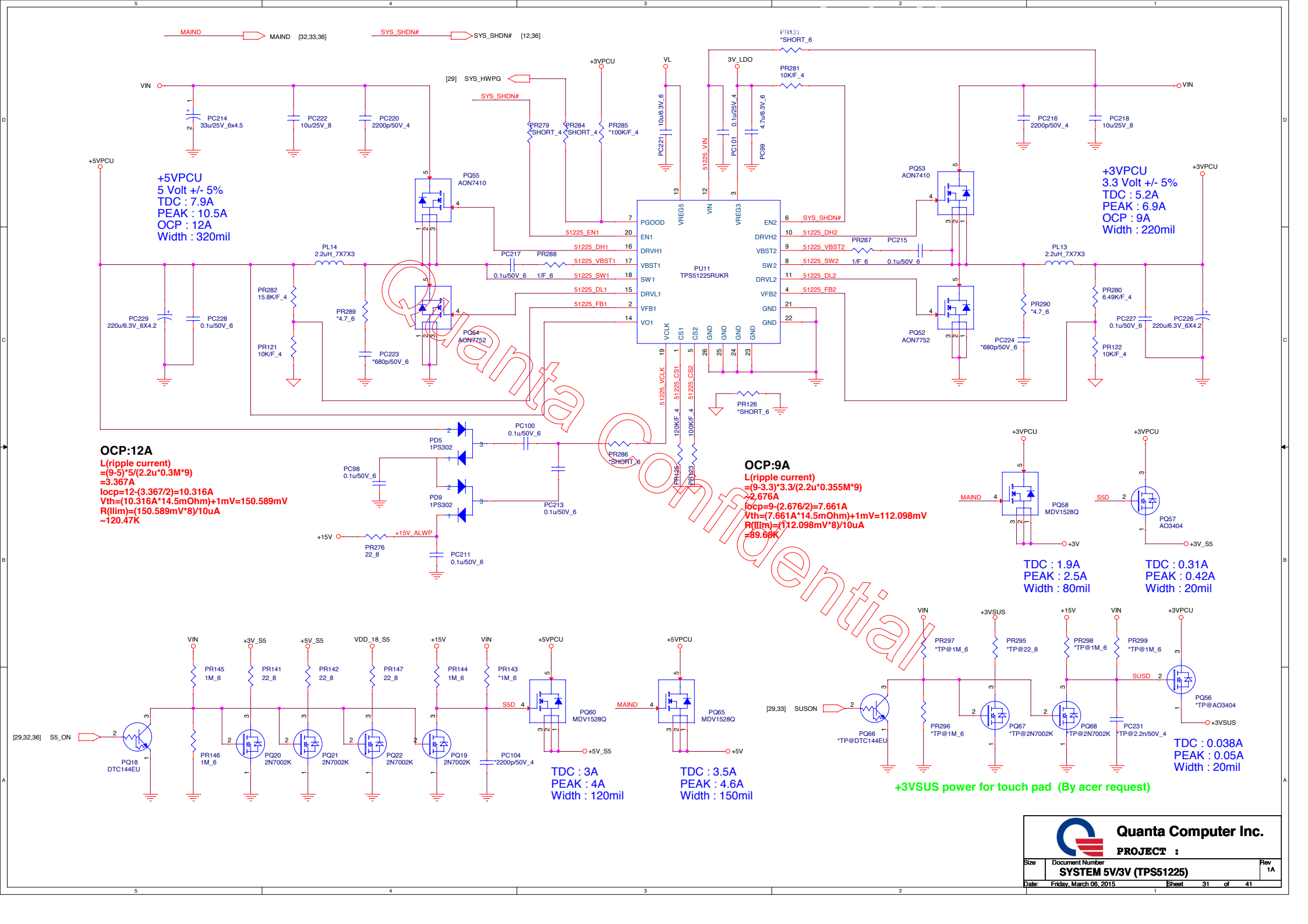
MAIND [32,33,36]
SYS_SHDN# [12,36]
[29] SYS_HWPG
+5VPCU
5 Volt +/- 5%
TDC : 7.9A
PEAK : 10.5A
OCP : 12A
Width : 320mil
+3VPCU
3.3 Volt +/- 5%
TDC : 5.2A
PEAK : 6.9A
OCP : 9A
Width : 220mil
PU11
TPS51225RUKR
OCP:12A
L(ripple current)
=(9-5)*5/(2.2u*0.3M*9)
=3.367A
Iocp=12-(3.367/2)=10.316A
Vth=(10.316A*14.5mOhm)+1mV=150.589mV
R(Ilim)=(150.589mV*8)/10uA
~120.47K
OCP:9A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.355M*9)
=2.676A
Iocp=9-(2.676/2)=7.661A
Vth=(7.661A*14.5mOhm)+1mV=112.098mV
R(Ilim)=(112.098mV*8)/10uA
=89.68K
TDC : 1.9A
PEAK : 2.5A
Width : 80mil
TDC : 0.31A
PEAK : 0.42A
Width : 20mil
TDC : 3A
PEAK : 4A
Width : 120mil
TDC : 3.5A
PEAK : 4.6A
Width : 150mil
TDC : 0.038A
PEAK : 0.05A
Width : 20mil
+3VSUS power for touch pad (By acer request)
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Quanta Computer Inc.
PROJECT :
SYSTEM 5V/3V (TPS51225)
Size
Document Number
Rev
1A
Date: Friday, March 06, 2015
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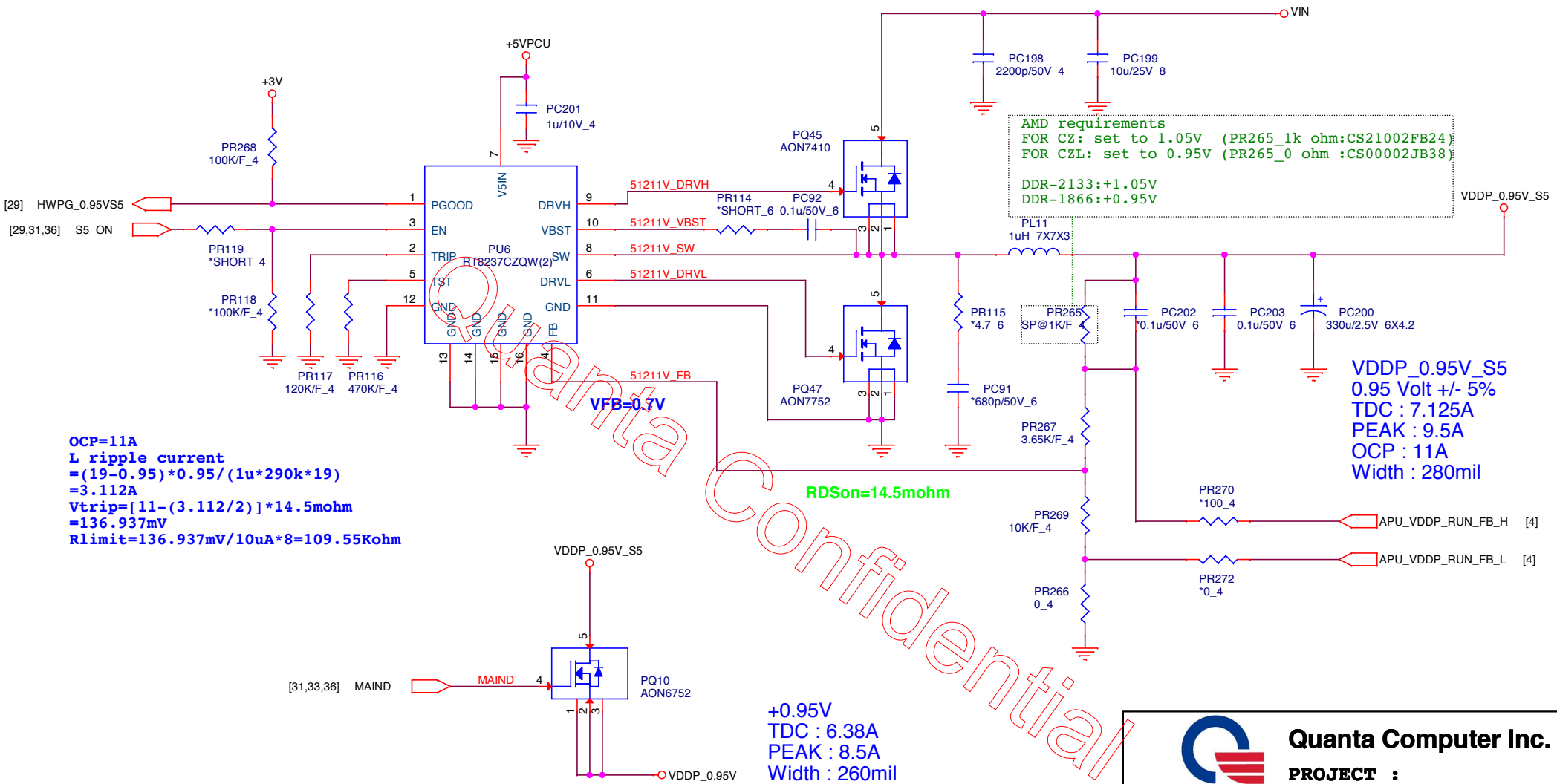

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Quanta Computer Inc.

PROJECT :

Size	Document Number	Rev
	VDDP_0.95V_S5 (RT8237CZQW)	1A

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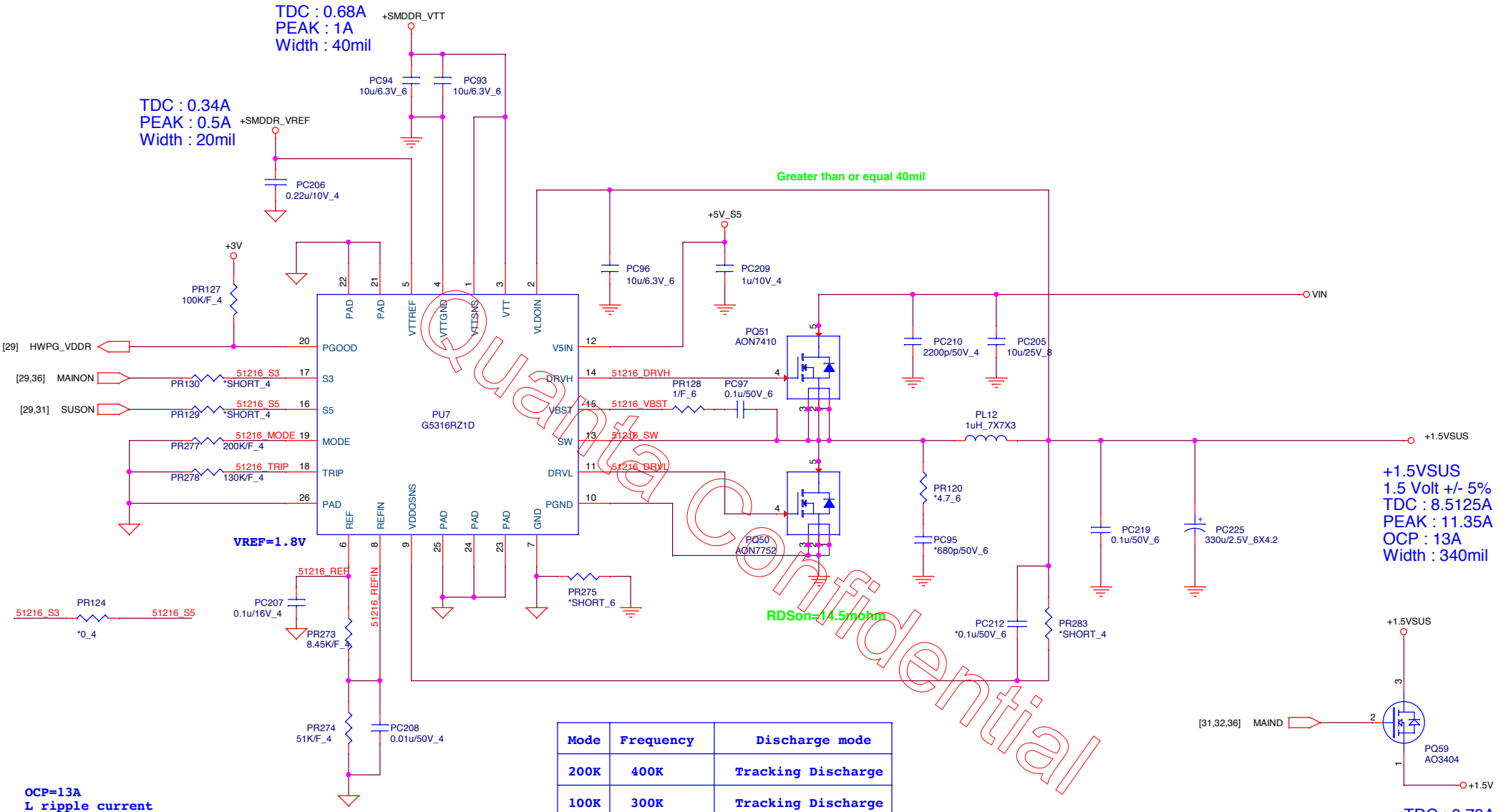

Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

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Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
	DDR3 1.5V (G5316RZ1D)	1A

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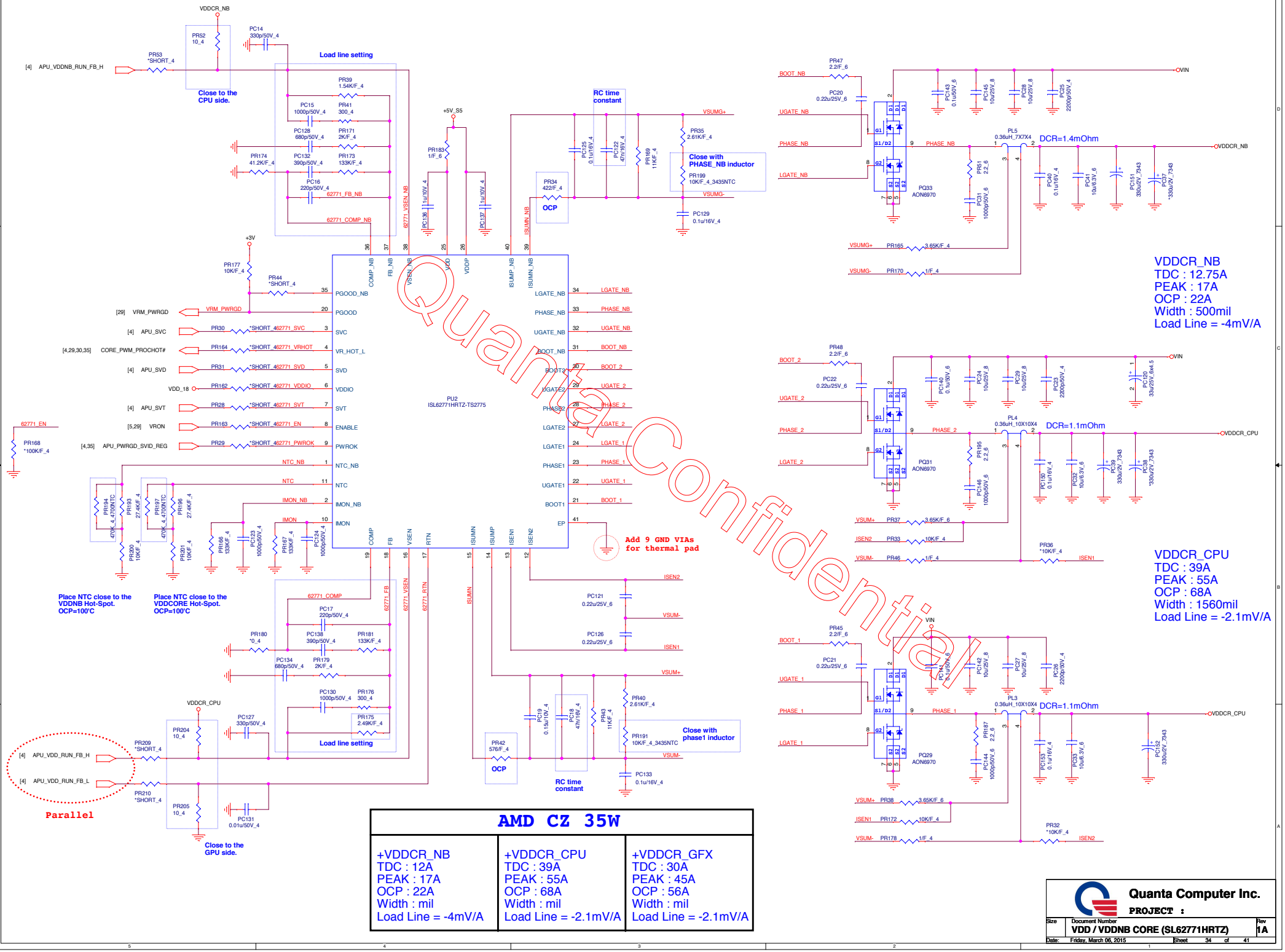

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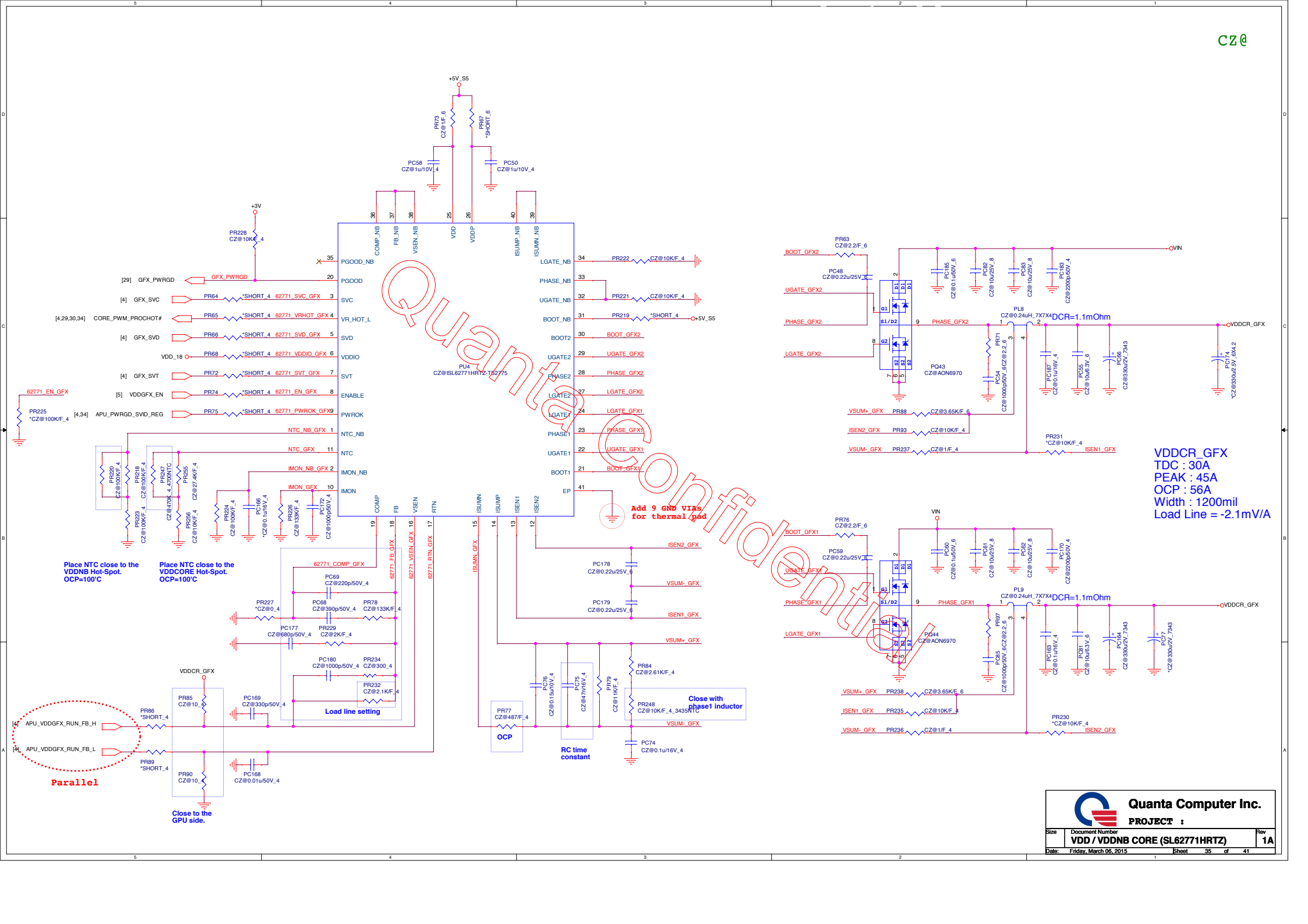
CZ@
+5V_S5
PR73 CZ@1/F_6
PR67 *SHORT_6
PC58 CZ@1u/10V_4
PC50 CZ@1u/10V_4
+3V
PR228 CZ@10K/F_4
PU4
CZ@ISL62771HRTZ-T52775
COMP_NB
FB_NB
VSEN_NB
VDD
VDDP
ISUMP_NB
ISUMN_NB
PGOOD_NB
PGOOD
SVC
VR_HOT_L
SVD
VDDIO
SVT
ENABLE
PWROK
NTC_NB
NTC
IMON_NB
IMON
LGATE_NB
PHASE_NB
UGATE_NB
BOOT_NB
BOOT2
UGATE2
PHASE2
LGATE2
LGATE1
PHASE1
UGATE1
BOOT1
EP
COMP
FB
VSEN
RTN
ISUMN
ISUMP
ISEN1
ISEN2
[29] GFX_PWRGD
[4] GFX_SVC
[4,29,30,34] CORE_PWM_PROCHOT#
[4] GFX_SVD
VDD_18
[4] GFX_SVT
[5] VDDGFX_EN
[4,34] APU_PWRGD_SVID_REG
62771_EN_GFX
PR225 *CZ@100K/F_4
PR64 *SHORT_4 62771_SVC_GFX
PR65 *SHORT_4 62771_VRHOT_GFX
PR66 *SHORT_4 62771_SVD_GFX
PR68 *SHORT_4 62771_VDDIO_GFX
PR72 *SHORT_4 62771_SVT_GFX
PR74 *SHORT_4 62771_EN_GFX
PR75 *SHORT_4 62771_PWROK_GFX
NTC_NB_GFX
NTC_GFX
IMON_NB_GFX
IMON_GFX
PR220 CZ@100K/F_4
PR218 CZ@100K/F_4
PR247 CZ@470K_4 4700NTC
PR255 CZ@27.4K/F_4
PR223 CZ@100K/F_4
PR256 CZ@10K/F_4
PR224 CZ@100K/F_4
PC166 *CZ@0.1u/16V_4
PR225 CZ@133K/F_4
PC172 CZ@1000p/50V_4
Place NTC close to the VDDNB Hot-Spot. OCP=100'C
Place NTC close to the VDDCORE Hot-Spot. OCP=100'C
62771_COMP_GFX
62771_FB_GFX
62771_VSEN_GFX
62771_RTN_GFX
ISUMN_GFX
PC69 CZ@220p/50V_4
PR227 *CZ@0_4
PC68 CZ@390p/50V_4
PR78 CZ@133K/F_4
PC177 CZ@680p/50V_4
PR229 CZ@2K/F_4
PC180 CZ@1000p/50V_4
PR234 CZ@300_4
PR232 CZ@2.1K/F_4
Load line setting
PR222 CZ@10K/F_4
PR221 CZ@10K/F_4
PR219 *SHORT_4
+5V_S5
BOOT_GFX2
UGATE_GFX2
PHASE_GFX2
LGATE_GFX2
ISEN2_GFX
VSUM-_GFX
ISEN1_GFX
VSUM+_GFX
PC178 CZ@0.22u/25V_6
PC179 CZ@0.22u/25V_6
PR84 CZ@2.61K/F_4
PR248 CZ@10K/F_4_3435NTC
Close with phase1 inductor
PR77 CZ@487/F_4
OCP
PC76 CZ@0.15u/10V_4
PC75 CZ@47n/16V_4
PR79 CZ@11K/F_4
RC time constant
PC74 CZ@0.1u/16V_4
Add 9 GND VIAs for thermal pad
VDDCR_GFX
PR85 CZ@10_4
PR86 *SHORT_4
PC169 CZ@330p/50V_4
[4] APU_VDDGFX_RUN_FB_H
[4] APU_VDDGFX_RUN_FB_L
PR89 *SHORT_4
PR90 CZ@10_4
PC168 CZ@0.01u/50V_4
Parallel
Close to the GPU side.
VIN
PR63 CZ@2.2/F_6
PC48 CZ@0.22u/25V_6
PC165 CZ@0.1u/50V_6
PC82 CZ@10u/25V_8
PC83 CZ@10u/25V_8
PC183 CZ@220p/50V_4
PL8 CZ@0.24uH_7X7X4 DCR=1.1mOhm
PQ43 CZ@AON6970
PR71 CZ@2.2_6
PC54 CZ@1000p/50V_6CZ@2.2_6
PC187 CZ@0.1u/16V_4
PC55 CZ@10u/6.3V_6
PC56 CZ@330u/2V_7343
PC174 *CZ@330u/2.5V_6X4.2
VSUM+_GFX PR88 CZ@3.65K/F_6
ISEN2_GFX PR93 CZ@10K/F_4
VSUM-_GFX PR237 CZ@1/F_4
PR231 *CZ@10K/F_4
VDDCR_GFX
TDC : 30A
PEAK : 45A
OCP : 56A
Width : 1200mil
Load Line = -2.1mV/A
PR76 CZ@2.2/F_6
PC59 CZ@0.22u/25V_6
PC60 CZ@0.1u/50V_6
PC61 CZ@10u/25V_8
PC62 CZ@10u/25V_8
PC170 CZ@220p/50V_4
PL9 CZ@0.24uH_7X7X4 DCR=1.1mOhm
PQ44 CZ@AON6970
PR97 CZ@2.2_6
PC35 CZ@1000p/50V_6CZ@2.2_6
PC163 CZ@0.1u/16V_4
PC51 CZ@10u/6.3V_6
PC164 CZ@330u/2V_7343
PC77 *CZ@330u/2V_7343
VSUM+_GFX PR238 CZ@3.65K/F_6
ISEN1_GFX PR235 CZ@10K/F_4
VSUM-_GFX PR236 CZ@1/F_4
PR230 *CZ@10K/F_4
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Quanta Computer Inc.
PROJECT :
Size
Document Number
VDD / VDDNB CORE (SL62771HRTZ)
Rev 1A
Date: Friday, March 06, 2015
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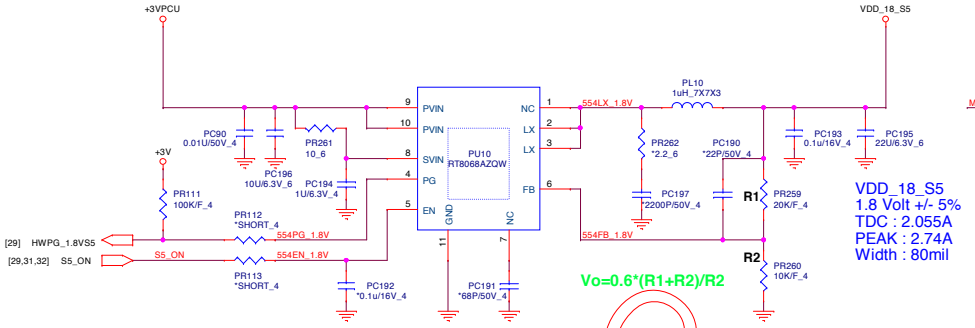

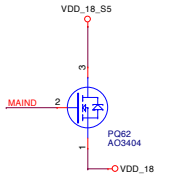

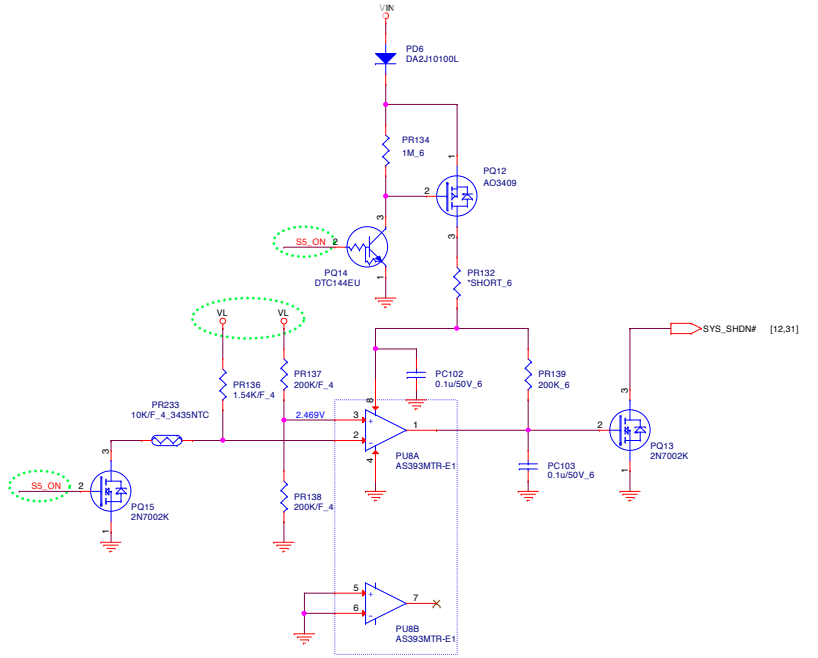

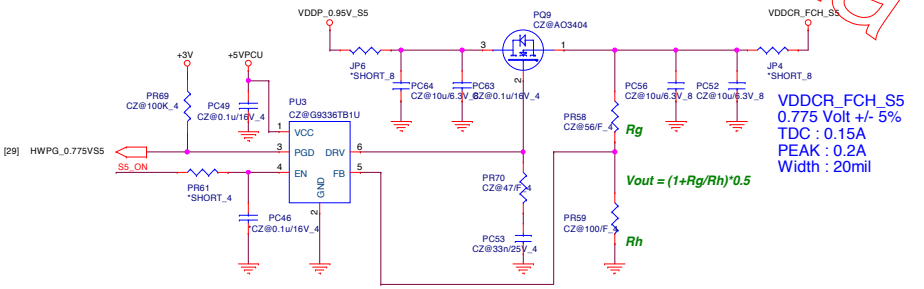

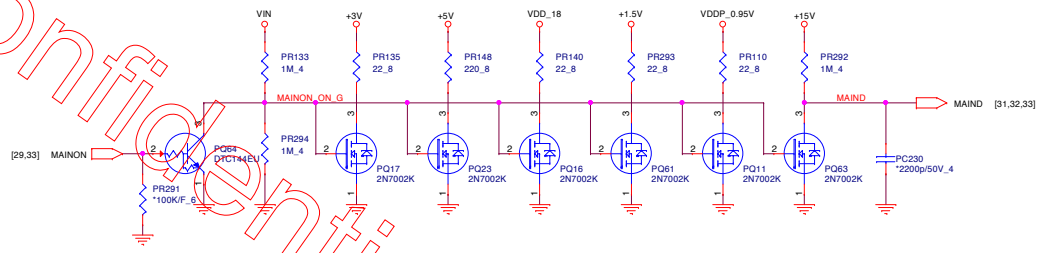

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	+1.8V/Thermal	1A

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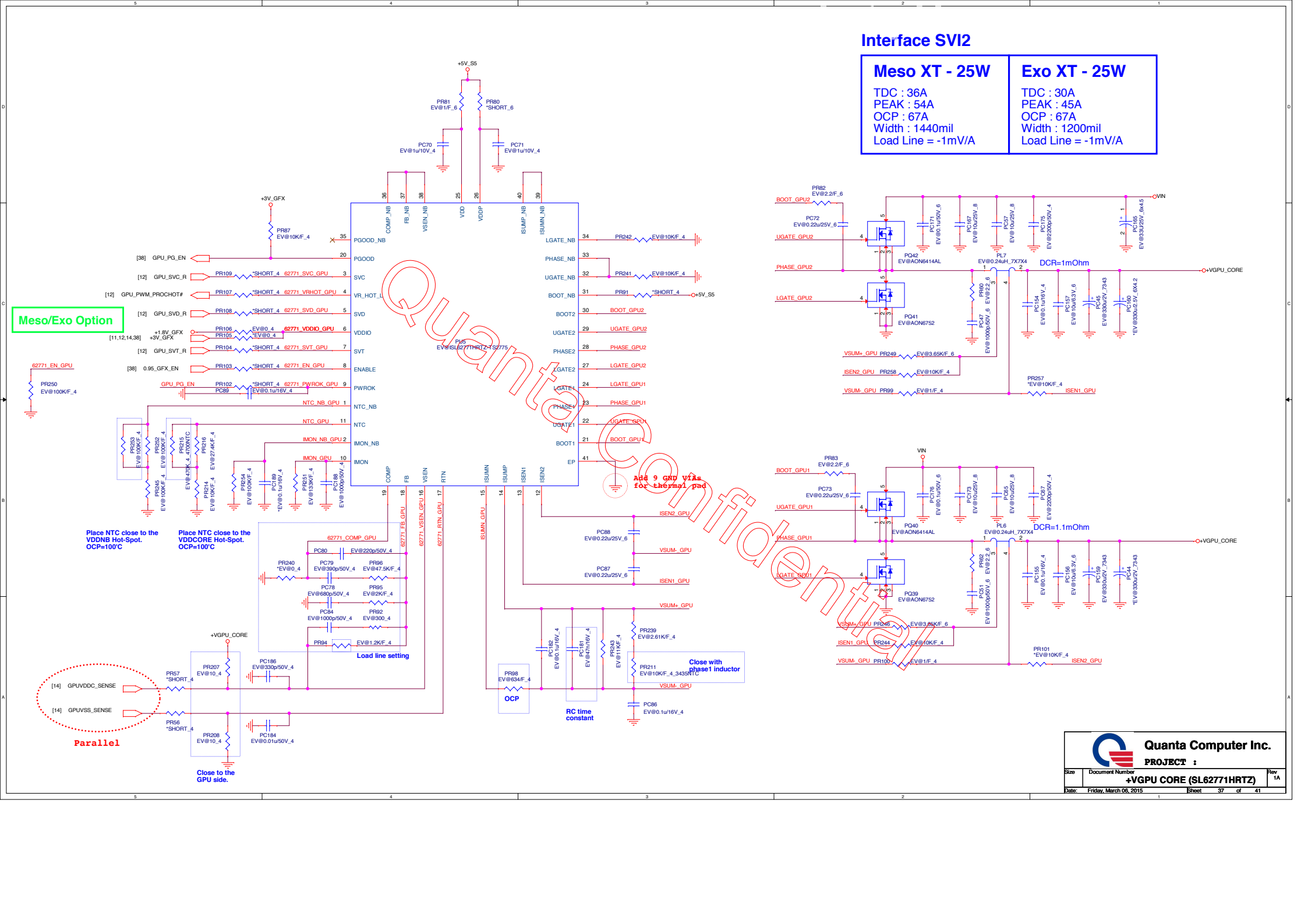
Interface SVI2
Meso XT - 25W
TDC : 36A
PEAK : 54A
OCP : 67A
Width : 1440mil
Load Line = -1mV/A
Exo XT - 25W
TDC : 30A
PEAK : 45A
OCP : 67A
Width : 1200mil
Load Line = -1mV/A
Meso/Exo Option
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PU5
EV@ISL62771HRTZ-T3775
DCR=1mOhm
DCR=1.1mOhm
Place NTC close to the VDDNB Hot-Spot. OCP=100'C
Place NTC close to the VDDCORE Hot-Spot. OCP=100'C
Add 9 GND vias for thermal pad
Load line setting
OCP
RC time constant
Close with phase1 inductor
Parallel
Close to the GPU side.
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PROJECT :
+VGPU CORE (SL62771HRTZ)
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Rev 1A
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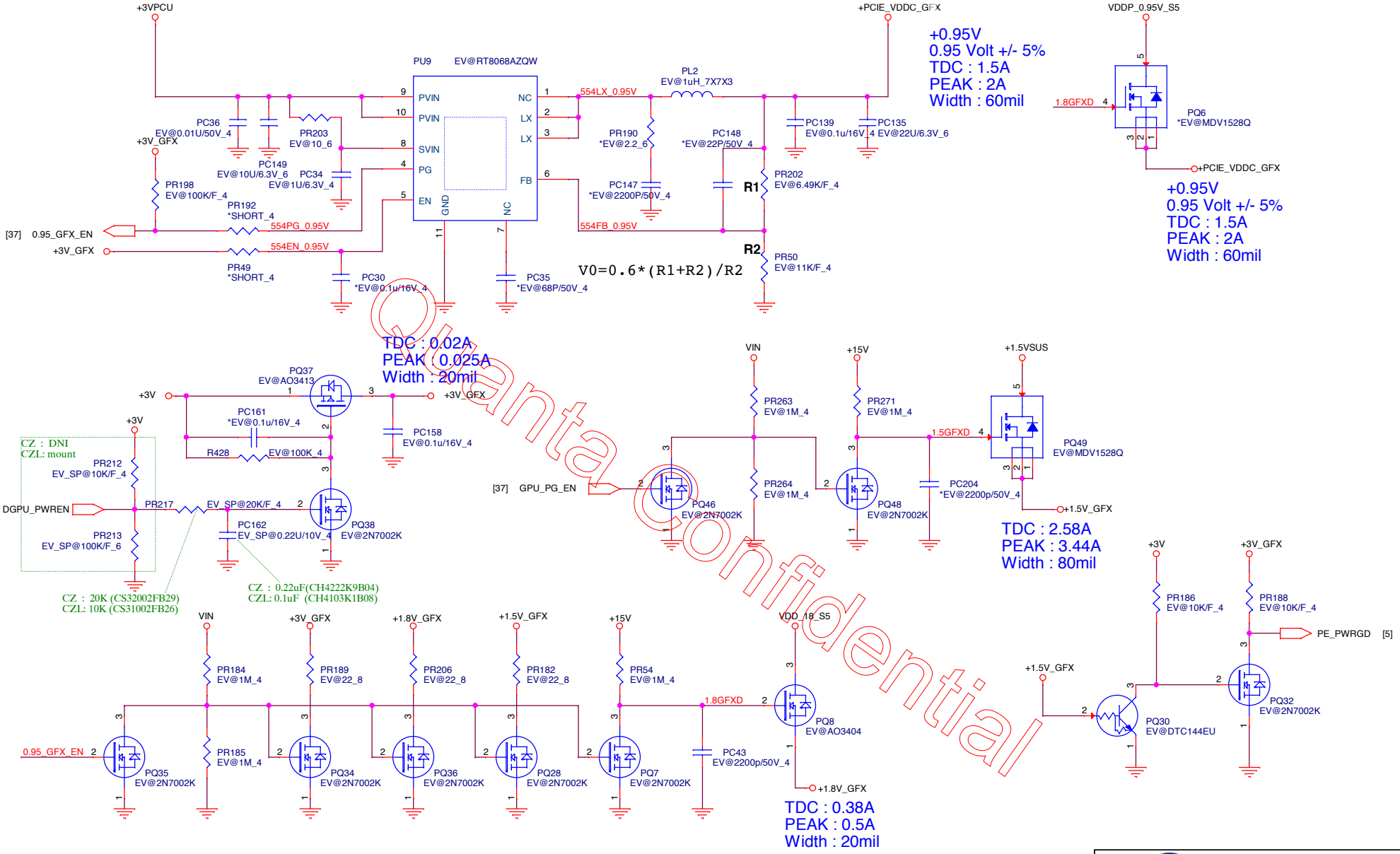

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PROJECT :		
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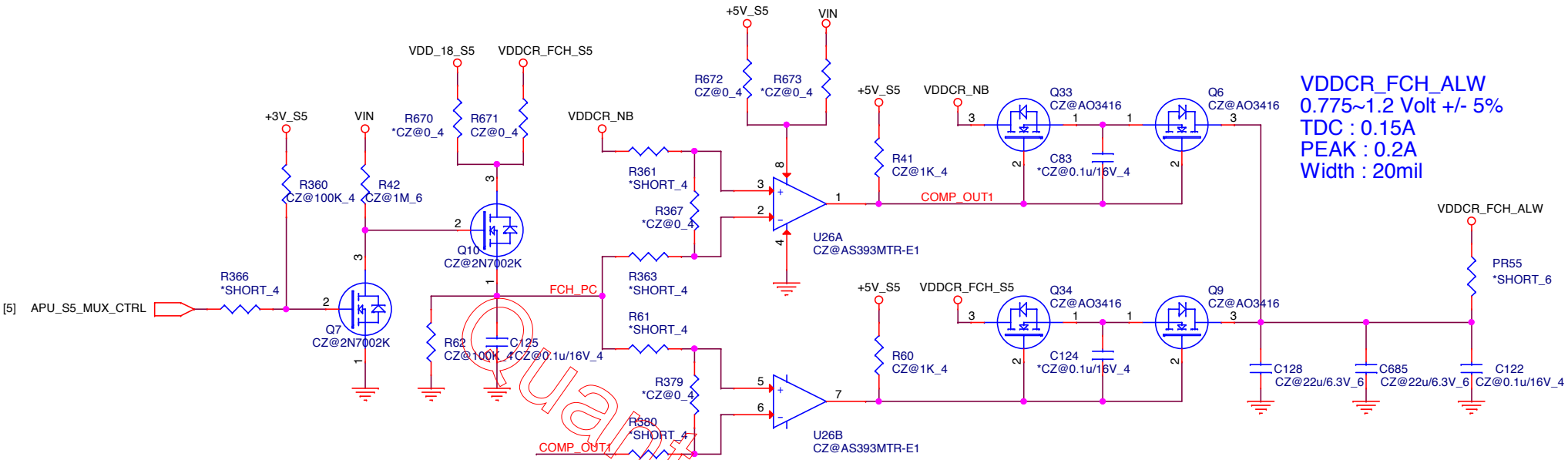

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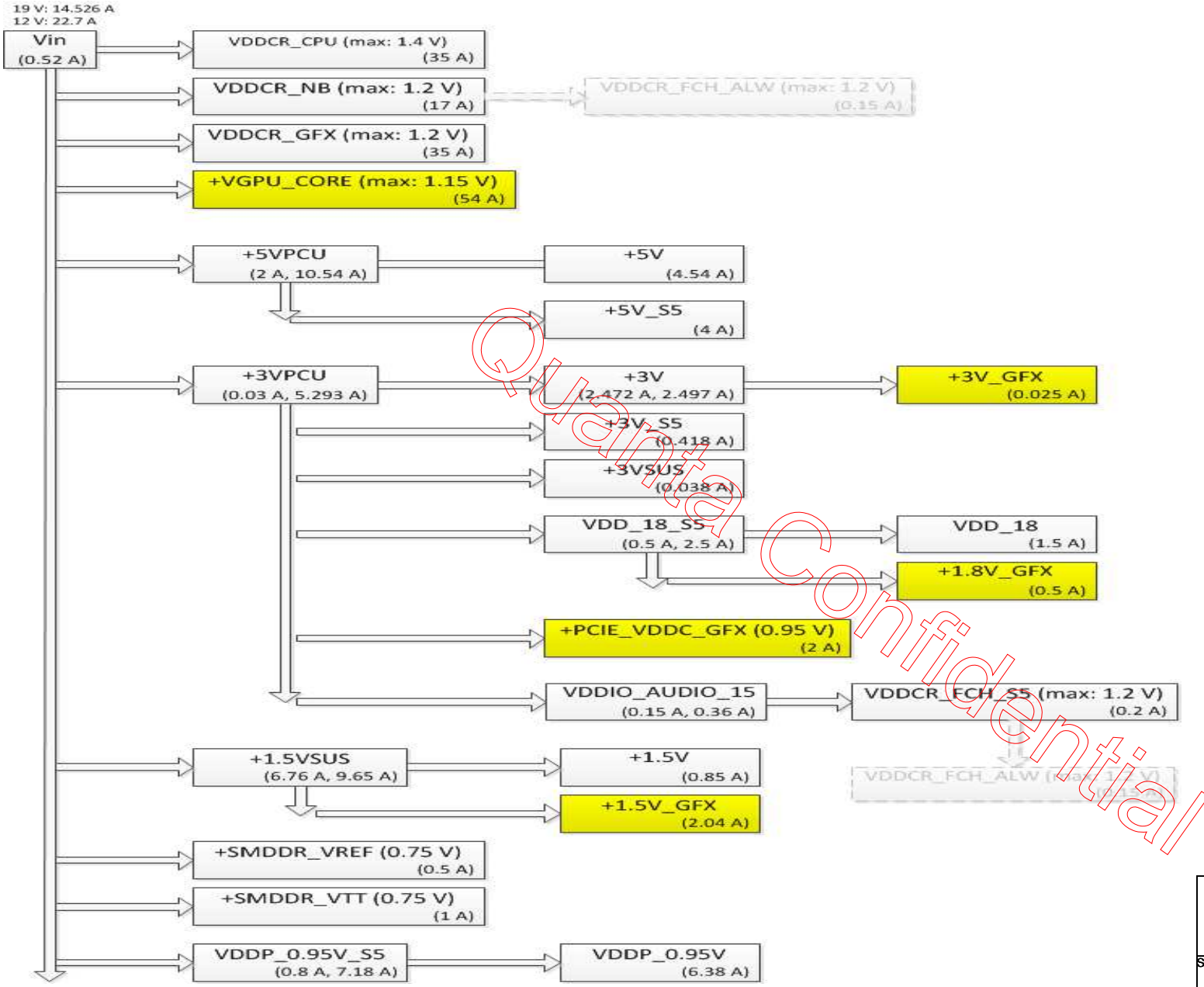
PROJECT :		
Size	Document Number: VDDCR_FCH_ALW	Rev: 1A
Date: Friday, March 06, 2015	Sheet 39 of 41	



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PROJECT :

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	Power tree	1A

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